The SN74LS16 is obsolete and is no longer supplied.

- **Convert TTL Voltage Levels to MOS Levels**
- **High Sink-Current Capability**
- **Input Clamping Diodes Simplify System Design**
- **Open-Collector Driver for Indicator Lamps and Relays**
- **Inputs Fully Compatible With Most TTL Circuits**

description/ordering information

These hex inverter buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The 'LS06 devices have a rated output voltage of 30 V, and the SN74LS16 has a rated output voltage of 15 V. The maximum sink current for the SN54LS06 is 30 mA, and for the SN74LS06 and SN74LS16 it is 40 mA.

These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

SN54LS06 . . . J PACKAGE
SN74LS06, SN74LS16 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)

```
      ┌───────┐
1A  [ 1      14 ] V_CC
1Y  [ 2      13 ] 6A
2A  [ 3      12 ] 6Y
2Y  [ 4      11 ] 5A
3A  [ 5      10 ] 5Y
3Y  [ 6       9 ] 4A
GND [ 7       8 ] 4Y
      └───────┘
```

SN54LS06 . . . FK PACKAGE
(TOP VIEW)

```
           1Y  1A  NC  V_CC 6A
            3   2   1   20  19
2A  [ 4                    18 ] 6Y
NC  [ 5                    17 ] NC
2Y  [ 6                    16 ] 5A
NC  [ 7                    15 ] NC
3A  [ 8                    14 ] 5Y
            9  10  11  12  13
           3Y  GND NC  4Y  4A
```

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS06N	SN74LS06N
	SOIC – D	Tube	SN74LS06D	LS06
		Tape and reel	SN74LS06DR	
	SOP – NS	Tape and reel	SN74LS06NSR	74LS06
	SSOP – DB	Tape and reel	SN74LS06DBR	LS06
–55°C to 125°C	CDIP – J	Tube	SN54LS06J	SN54LS06J
		Tube	SNJ54LS06J	SNJ54LS06J
	LCCC – FK	Tube	SNJ54LS06FK	SNJ54LS06FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54LS06, SN74LS06, SN74LS16
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS
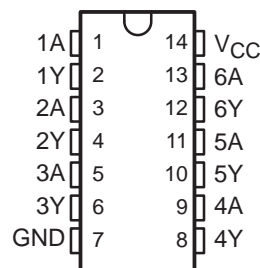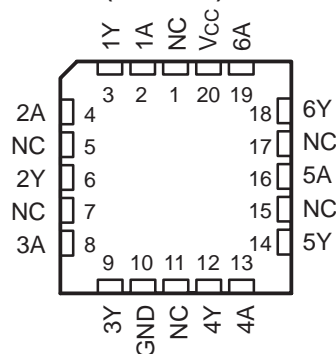SDLS020E – MAY 1990 – REVISED FEBRUARY 2004

**The SN74LS16 is obsolete
and is no longer supplied.**

logic diagram (positive logic)
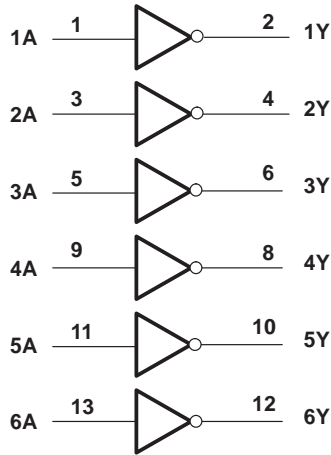
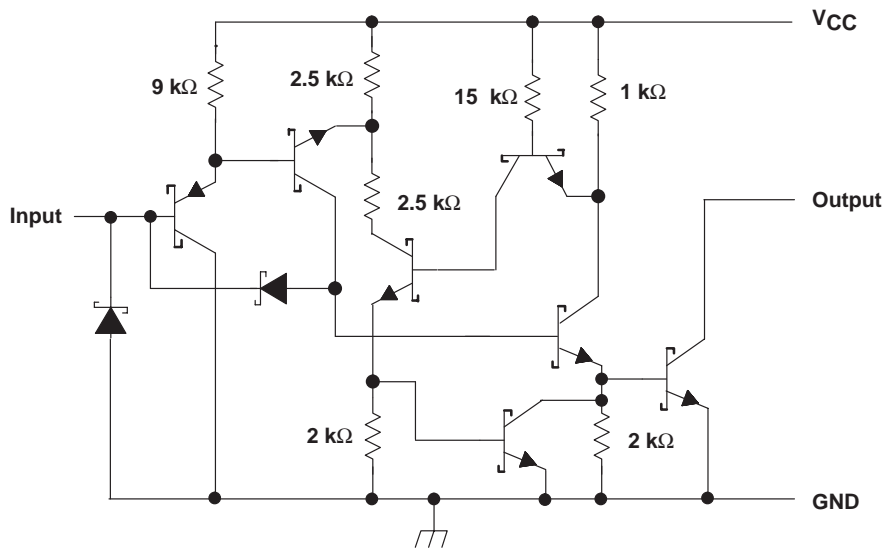Pin numbers shown are for the D, DB, J, N, and NS packages.

schematic (each gate)

Resistor values shown are nominal.

**The SN74LS16 is obsolete
and is no longer supplied.**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I (see Note 1) .... 7 V
Output voltage, V_O (see Notes 1 and 2): SN54LS06, SN74LS06 .... 30 V
SN74LS16 .... 15 V
Package thermal impedance, θ_{JA} (see Note 3): D package .... 86°C/W
DB package .... 96°C/W
N package .... 80°C/W
NS package .... 76°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to GND.
        2. This is the maximum voltage that should be applied to any output when it is in the off state.
        3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LS06			SN74LS06 SN74LS16			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	'LS06			30			30	V
		SN74LS16						15	
I_{OL}	Low-level output current				30			40	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		SN54LS06			SN74LS06 SN74LS16			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V	'LS06, V_{OH} = 30 V			0.25			0.25	mA
		SN74LS16, V_{OH} = 15 V						0.25	
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 16 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 30 mA			0.7				
		I_{OL} = 40 mA						0.7	
I_I	V_{CC} = MAX, V_I = 7 V				1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				20			20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{CCH}	V_{CC} = MAX				18			18	mA
I_{CCL}	V_{CC} = MAX				60			60	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under *recommended operating conditions*.
§ All typical values are at V_{CC} = 5 V, and T_A = 25°C.

**TEXAS
INSTRUMENTS**

SN54LS06, SN74LS06, SN74LS16
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS
SDLS020E – MAY 1990 – REVISED FEBRUARY 2004

**The SN74LS16 is obsolete
and is no longer supplied.**

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

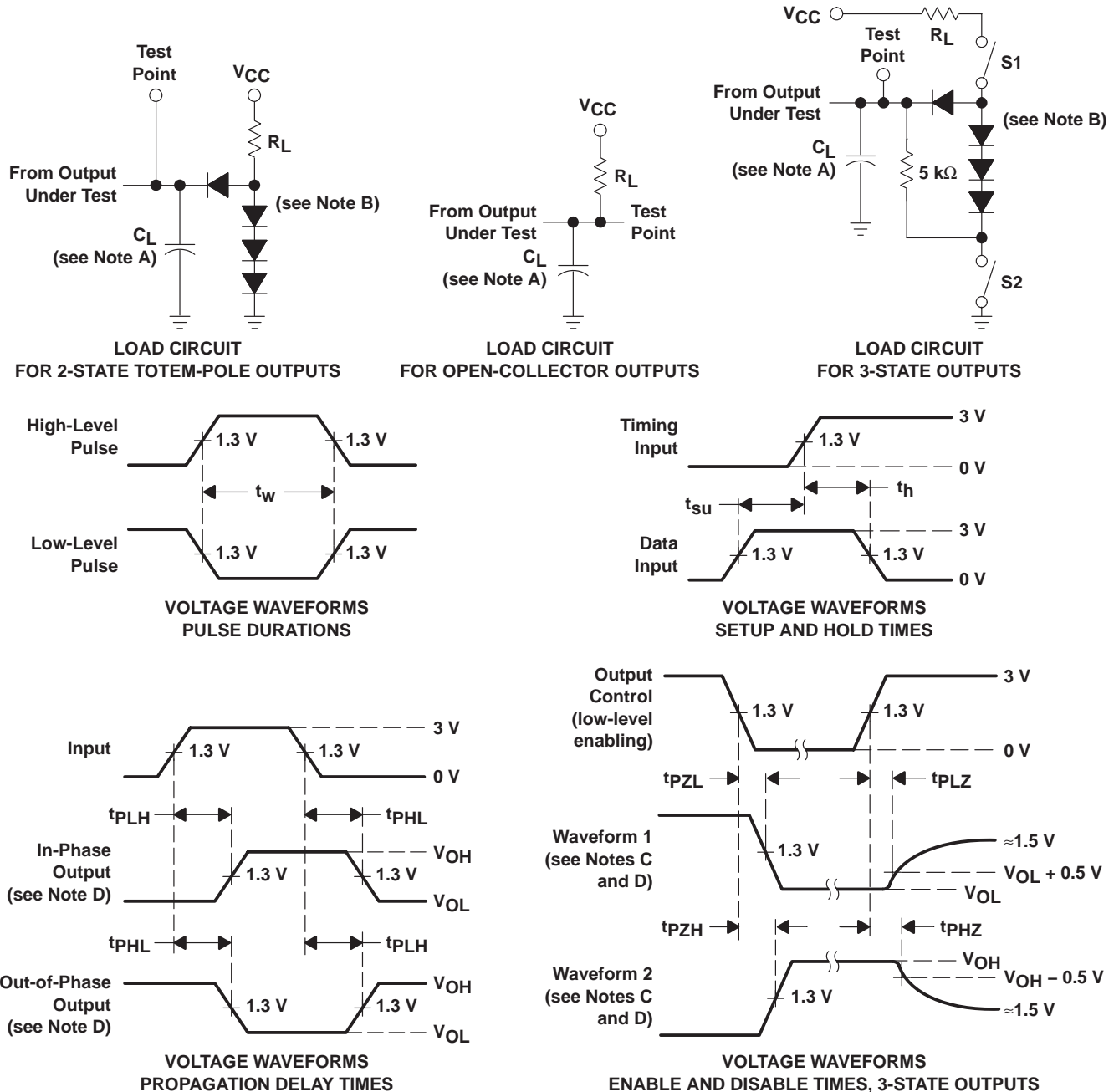| PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω,	C_L = 15 pF	7	15	ns
t_{PHL}					10	20	

**The SN74LS16 is obsolete
and is no longer supplied.**

PARAMETER MEASUREMENT INFORMATION

Test Point

V$_{CC}$

R$_L$

From Output Under Test

(see Note B)

C$_L$
(see Note A)

**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**

V$_{CC}$

R$_L$

From Output Under Test

Test Point

C$_L$
(see Note A)

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

V$_{CC}$

Test Point

R$_L$

S1

From Output Under Test

(see Note B)

C$_L$
(see Note A)

5 kΩ

S2

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

High-Level Pulse

1.3 V   1.3 V

t$_w$

Low-Level Pulse

1.3 V   1.3 V

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

Timing Input

3 V

1.3 V

0 V

t$_{su}$ t$_h$

Data Input

3 V

1.3 V   1.3 V

0 V

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

Input

3 V

1.3 V   1.3 V

0 V

t$_{PLH}$ t$_{PHL}$

In-Phase Output
(see Note D)

V$_{OH}$

1.3 V   1.3 V

V$_{OL}$

t$_{PHL}$ t$_{PLH}$

Out-of-Phase Output
(see Note D)

V$_{OH}$

1.3 V   1.3 V

V$_{OL}$

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**Output Control
(low-level enabling)**

3 V

1.3 V   1.3 V

0 V

t$_{PZL}$ t$_{PLZ}$

**Waveform 1
(see Notes C and D)**

≈1.5 V

1.3 V

V$_{OL}$ + 0.5 V

V$_{OL}$

t$_{PZH}$ t$_{PHZ}$

**Waveform 2
(see Notes C and D)**

V$_{OH}$

1.3 V

V$_{OH}$ – 0.5 V

≈1.5 V

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C$_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for t$_{PLH}$, t$_{PHL}$, t$_{PHZ}$, and t$_{PLZ}$; S1 is open and S2 is closed for t$_{PZH}$; S1 is closed and S2 is open for t$_{PZL}$.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z$_O$ ≈ 50 Ω, t$_r$ ≤ 1.5 ns, t$_f$ ≤ 2.6 ns.
G. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9861701Q2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9861701QCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54LS06J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN74LS06D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS06DBLE	OBSOLETE	SSOP	DB	14		None	Call TI	Call TI
SN74LS06DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS06DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS06N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS06NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS16D	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
SN74LS16DR	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
SN74LS16N	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SNJ54LS06FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS06J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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	PINS **	14	16	18	20
DIM					
A		0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B	MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B	MIN	——	——	——	——
C	MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C	MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

C

1   7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

A

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

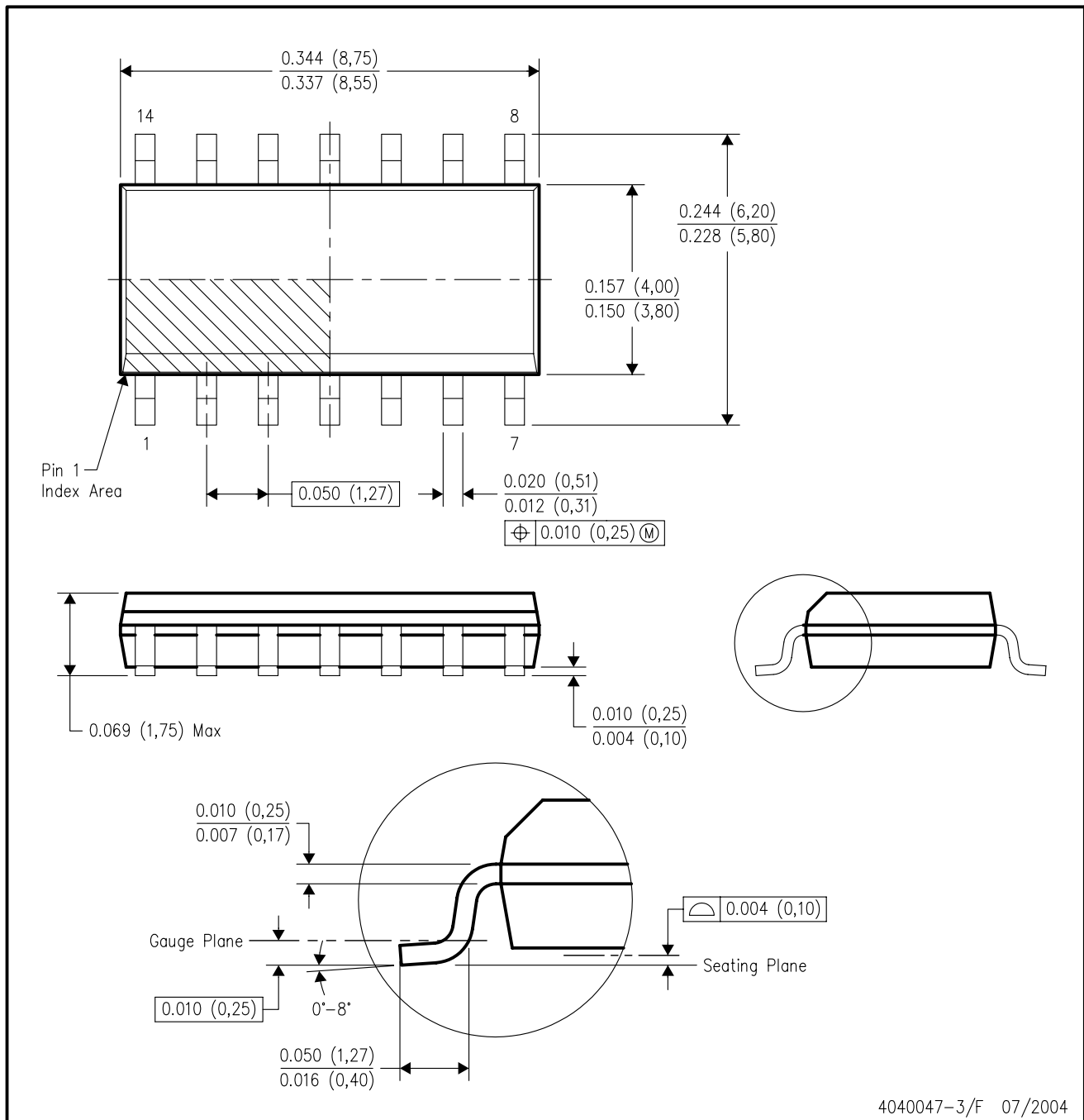0.100 (2,54)

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

FK (S-CQCC-N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F   07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM	PINS ** 14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

IMPORTANT NOTICE

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless