LPC-H2124 HEADER BOARD FOR LPC2124 ARM7TDMI-S MICROCONTROLLER

Features:

- MCU: LPC2124 16/32 bit ARM7TDMI-S™ with 256K Bytes Program Flash, 16K Bytes RAM, RTC, 4x 10 bit ADC 2.44 uS, 2x UART, I2C, SPI, 2x 32bit TIMERS, 7x CCR, 6x PWM, WDT, 5V tolerant I/O, up to 60MHz operation
- standard JTAG connector with ARM 2x10 pin layout for programming/debugging with ARM-JTAG
- two on board voltage regulators 1.8V and 3.3V with up to 800mA current
- single power supply: +5VDC required
- power supply status LED
- power supply filtering capacitor
- RESET circuit with external control of Philips ISP utility via RS232
- RESET button
- DBG jumper for JTAG enable
- BSL jumper for Bootloader enable
- JRST jumper for enable/disable external RESET control by RS232
- 10 Mhz crystal
- extension headers for all uC ports
- PCB: FR-4, 1.5 mm (0,062"), green soldermask, white silkscreen component print
- Dimensions: 76x55 mm (3.0x2.2")
- space between the pin rows: 48.26 mm (1.9")

Supported devices:

Philips Semiconductors Inc. LPC2124 16/32 bit ARM7TDMI-S™

JTAG interface:

The JTAG connector is 2x10 pin with 0,1" step and ARM recommended JTAG layout. PIN.1 is marked with square pad on bottom and arrow on top.

Note: to enable JTAG interface DBG jumper should be shorted at the time of POWER UP.

Important: when JTAG is enabled P1.16-P1.31 ports take their JTAG alternative function no matter of PINSEL1 register value, so during debugging with JTAG these ports are not available for the user program.

JTAG signals description:

PIN.1 (VTREF) Target voltage sense. Used to indicate the target's operating voltage to the debug tool.

PIN.2 (VTARGET) Target voltage. May be used to supply power to the debug tool.

PIN.3 (nTRST) JTAG TAP reset, this signal should be pulled up to Vcc in target board.

PIN4,6, 8, 10,12,14,16,18,20 Ground. The Gnd-Signal-Gnd-Signal strategy implemented on the 20-way connection scheme improves noise immunity on the target connect cable.

PIN.5 (TDI) JTAG serial data in, should be pulled up to Vcc on target board.

PIN.7 (TMS) JTAG TAP Mode Select, should be pulled up to Vcc on target board.

PIN.9 (TCK) JTAG clock.

PIN.11 (RTCK) JTAG re-timed clock. Implemented on certain ASIC ARM implementations the host ASIC may need to synchronize external inputs (such as JTAG inputs) with its own internal clock.

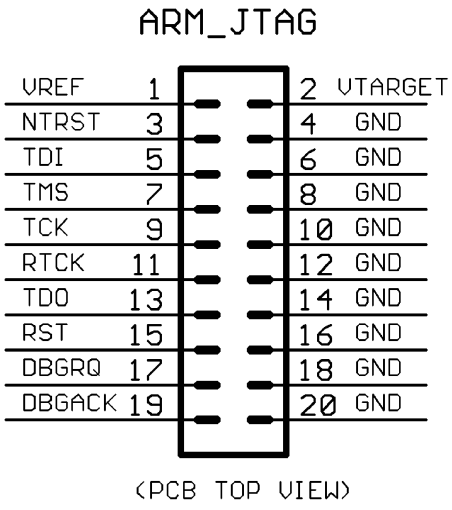
PIN.13 (TDO) JTAG serial data out.

PIN.15 (nSRST) Target system reset.

PIN.17 (DBGRQ) Asynchronous debug request. DBGRQ allows an external signal to force the ARM core into debug mode, should be pull down to GND.

PIN.19 (DBGACK) Debug acknowledge signal. The ARM core acknowledges debug-mode in response to a DBGRQ input.

JTAG connector layout:



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Power supply:
Power supply is made with two LDO adjustable voltage regulators LM1117. Input voltage should be in range 5-9VDC. Watch out the polarity as schematic have no input protection diode and reversing the input power supply will be fatal for LPC2124 microcontroller

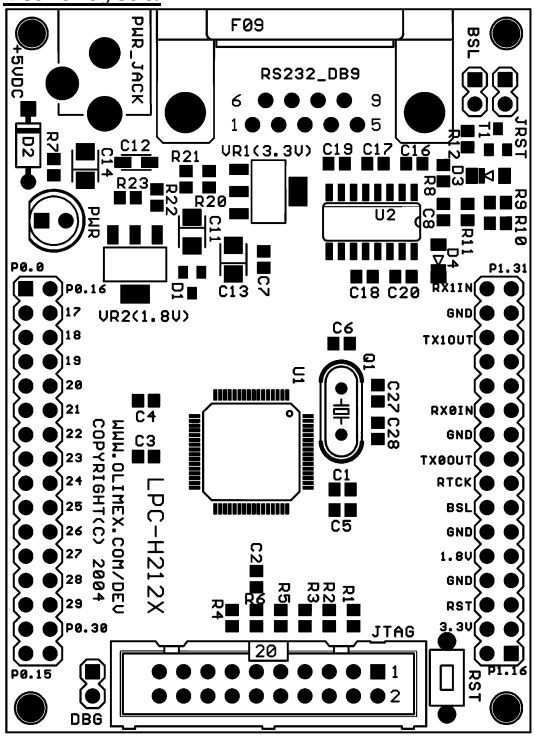
RS232 interface:
LPC2124 have two RS232 channels. They both are connected via MAX3232 IC and are available for use with RS232 levels. Channel 0 with TXD0 and RXD0 is used by the Bootloader program to program LPC2124 Flash memory without external programmer. Channel 1 is general purpose RS232 channel and may be used by user program. Channel 0 signals are available on SUB_D 9 pin connector.

RESET:
Reset circuit is made by simple external RC group. There is possibility to apply RESET externally via RS232 DTR signal (when JRST is shorted this feature is enabled) or by the small RESET pushbutton on the board.

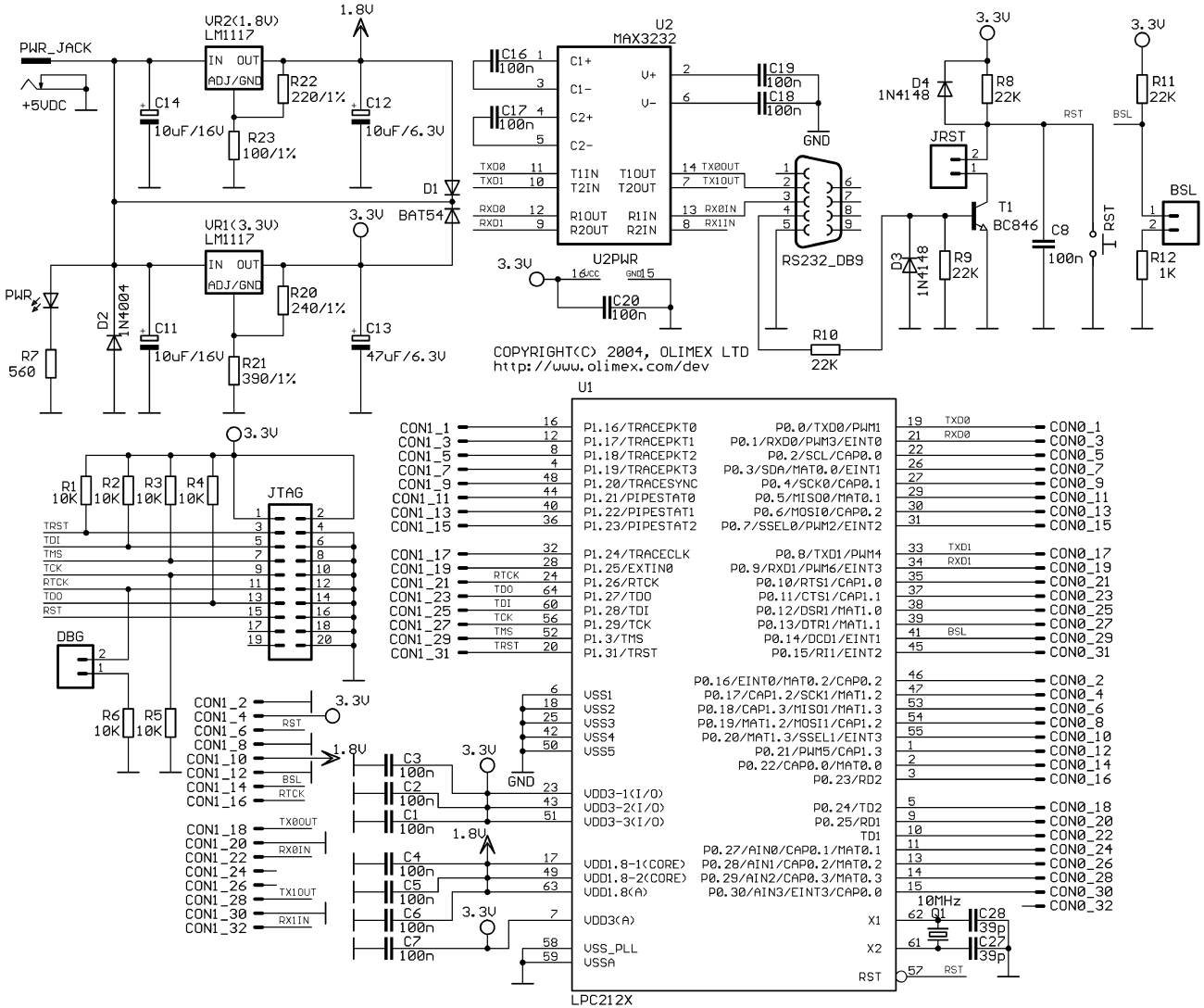
Oscillator:
According to LPC2124 datasheets internal PLL will work with external crystal in range 10-25Mhz, however our test with 14.7456 Mhz crystal show that JTAG communication doesn't work properly on devices with above 10Mhz external crystal, so despite 14.7456Mhz crystal allows very convenient communication values we had to install 10Mhz crystal for this device. This makes programming with Philips ISP utility above 38400 bps impossible, but JTAG debugger works without problems, switching crystal to 14.7456Mhz makes ISP programming possible at higher speeds like 115Kbps but JTAG debugger works unreliable.

Bootloader:
The Bootloader program is enabled when BSL jumper is shorted at time of power up. In this case Bootloader takes the program control and user may download Flash memory with Philips ISP programming utility. Note that if you want to run code in Flash memory BSL jumper should be open at time of power up, otherwise Bootloader will stay in control and will not allow program in Flash to run. The newer versions of Philips ISP utility use DTR signal as RESET control, if you want to use this feature jumper JRST should be shorted otherwise leave it open. (we recommend you when you use bootloader with Philips ISP utility to close both BSL and JRST jumpers, and when you run your code to leave these jumpers open). ISP utility allows many programming speeds to be choosen but with the 10Mhz crystal it works only up to 38400 bps.

Board layout:



Ordering codes:
LPC-H2124 - assembled and tested with LPC2124 microcontroller


PWR_JACK
+5VDC
VR2(1.8V)
LM1117
IN OUT
ADJ/GND
R22
220/1%
C14
10uF/16V
R23
100/1%
C12
10uF/6.3V
1.8V
D1
BAT54
3.3V
VR1(3.3V)
LM1117
R20
240/1%
C11
10uF/16V
R21
390/1%
C13
47uF/6.3V
PWR
R7
560
D2
1N4004
U2
MAX3232
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
T1OUT
T2OUT
R1OUT
R2IN
C16
C17
C18
C19
C20
100n
TXD0
TXD1
RXD0
RXD1
TX0OUT
TX1OUT
RX0IN
RX1IN
U2PWR
VCC
GND
RS232_DB9
R10
22K
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D4
1N4148
R8
22K
JRST
T1
BC846
C8
100n
RST
D3
1N4148
R9
22K
R11
22K
BSL
R12
1K
U1
LPC212X
P1.16/TRACEPKT0
P1.17/TRACEPKT1
P1.18/TRACEPKT2
P1.19/TRACEPKT3
P1.20/TRACESYNC
P1.21/PIPESTAT0
P1.22/PIPESTAT1
P1.23/PIPESTAT2
P1.24/TRACECLK
P1.25/EXTIN0
P1.26/RTCK
P1.27/TDO
P1.28/TDI
P1.29/TCK
P1.3/TMS
P1.31/TRST
P0.0/TXD0/PWM1
P0.1/RXD0/PWM3/EINT0
P0.2/SCL/CAP0.0
P0.3/SDA/MAT0.0/EINT1
P0.4/SCK0/CAP0.1
P0.5/MISO0/MAT0.1
P0.6/MOSI0/CAP0.2
P0.7/SSEL0/PWM2/EINT2
P0.8/TXD1/PWM4
P0.9/RXD1/PWM6/EINT3
P0.10/RTS1/CAP1.0
P0.11/CTS1/CAP1.1
P0.12/DSR1/MAT1.0
P0.13/DTR1/MAT1.1
P0.14/DCD1/EINT1
P0.15/RI1/EINT2
P0.16/EINT0/MAT0.2/CAP0.2
P0.17/CAP1.2/SCK1/MAT1.2
P0.18/CAP1.3/MISO1/MAT1.3
P0.19/MAT1.2/MOSI1/CAP1.2
P0.20/MAT1.3/SSEL1/EINT3
P0.21/PWM5/CAP1.3
P0.22/CAP0.0/MAT0.0
P0.23/RD2
P0.24/TD2
P0.25/RD1
TD1
P0.27/AIN0/CAP0.1/MAT0.1
P0.28/AIN1/CAP0.2/MAT0.2
P0.29/AIN2/CAP0.3/MAT0.3
P0.30/AIN3/EINT3/CAP0.0
VSS1
VSS2
VSS3
VSS4
VSS5
VDD3-1(I/O)
VDD3-2(I/O)
VDD3-3(I/O)
VDD1.8-1(CORE)
VDD1.8-2(CORE)
VDD1.8(A)
VDD3(A)
VSS_PLL
VSSA
X1
X2
RST
10MHz
Q1
C28
C27
39p
CON1_1
CON1_2
CON1_3
CON1_4
CON1_5
CON1_6
CON1_7
CON1_8
CON1_9
CON1_10
CON1_11
CON1_12
CON1_13
CON1_14
CON1_15
CON1_16
CON1_17
CON1_18
CON1_19
CON1_20
CON1_21
CON1_22
CON1_23
CON1_24
CON1_25
CON1_26
CON1_27
CON1_28
CON1_29
CON1_30
CON1_31
CON1_32
CON0_1
CON0_2
CON0_3
CON0_4
CON0_5
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CON0_21
CON0_22
CON0_23
CON0_24
CON0_25
CON0_26
CON0_27
CON0_28
CON0_29
CON0_30
CON0_31
CON0_32
JTAG
DBG
R1
R2
R3
R4
10K
TRST
TDI
TMS
TCK
RTCK
TDO
RST
R6
R5
C3
C2
C1
C4
C5
C6
C7
100n
GND