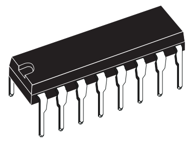
# HCF40110B

## DECADE UP/DOWN COUNTER/DECODER/LATCH/DRIVER

- SEPARATE CLOCK-UP AND CLOCK-DOWN LINES
- CAPABLE OF DRIVING COMMON CATHODE LEDS AND OTHER DISPLAYS DIRECTLY
- ALLOWS CASCADING WITHOUT ANY EXTERNAL CIRCUITRY
- MAXIMUM INPUT CURRENT OF 1 µA AT 18 V (full package-temperature range)
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTCS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT $I_I$ = 100nA (MAX) AT $V_{DD}$ = 18V $T_A$ = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

**ORDER CODES**

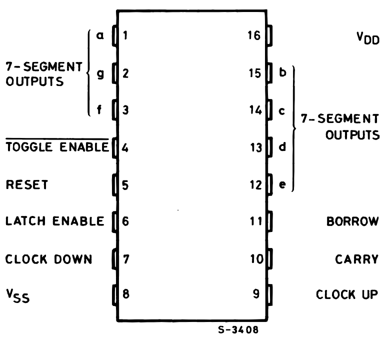
| PACKAGE | TUBE | T & R |
|---|---|---|
| DIP | HCF40110BEY | |

### DESCRIPTION

HCF40110B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.

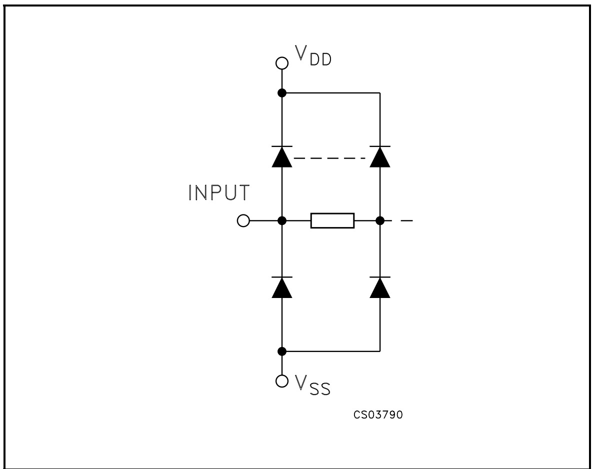
HCF40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of the states or timing (within 100 ns typ.) of the other clock line. The clock signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps. A short duration negative-going pulse appears on the BORROW output when the count changes from 0

### PIN CONNECTION



to 9 or the CARRY output when the count changes from 9 to 0. At other times the BORROW and BORROW outputs can be tied directly to the clock-up and clock-down lines, respectively, of another HCF40110B for easy cascading of several counters.

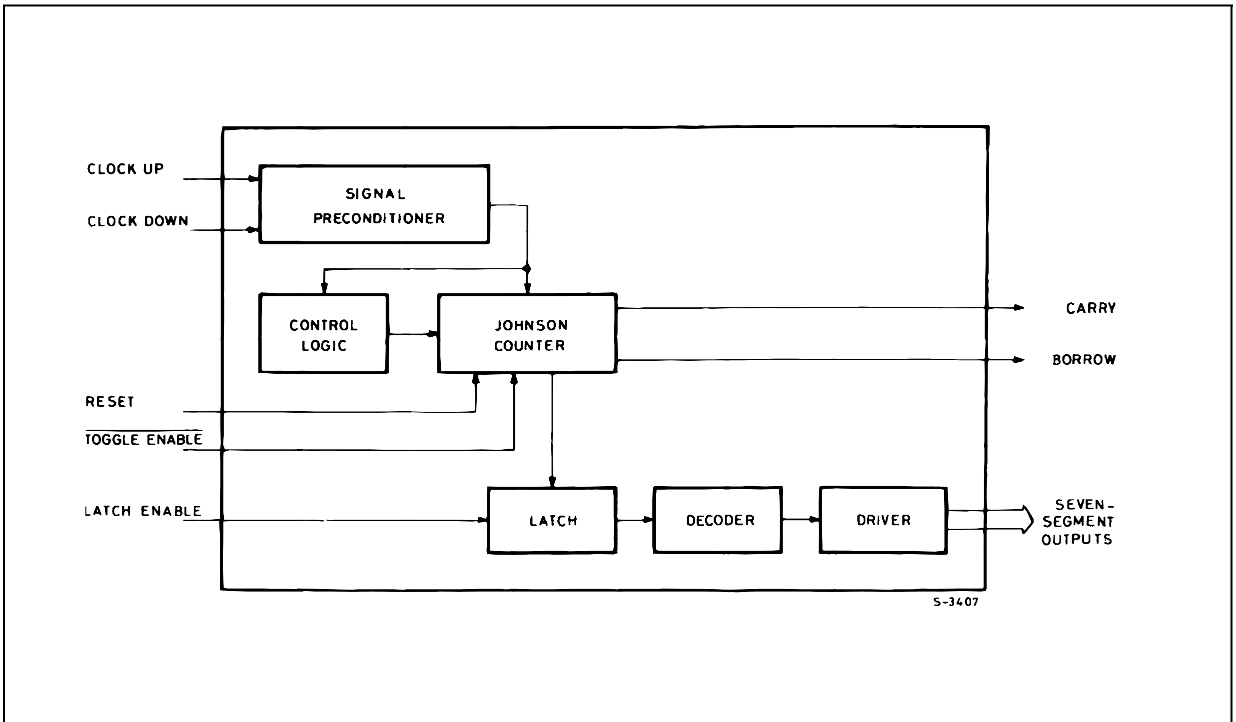
## INPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 15, 14, 13, 12, 3, 2 | a, b, c, d, e, f, g | 7 Segment Outputs |
| 4 | $\overline{\text{Toggle Enable}}$ | Enable Johnson Counter |
| 5 | Reset | Reset Input |
| 6 | Latch Enable | Latch Enable |
| 7 | Clock Down | Clock Down |
| 9 | Clock Up | Clock Up |
| 10 | Carry | Carry Output |
| 11 | Borrow | Borrow Output |
| 8 | $V_{SS}$ | Negative Supply Voltage |
| 16 | $V_{DD}$ | Positive Supply Voltage |

## FUNCTIONAL DIAGRAM (One Half)

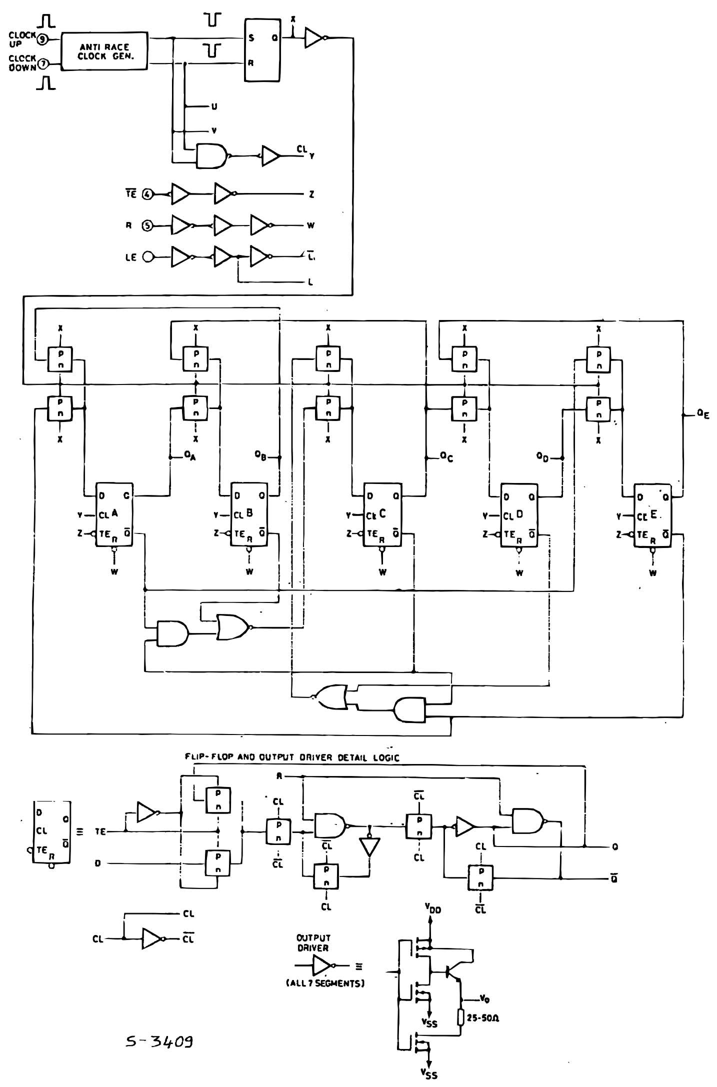


## TRUTH TABLES

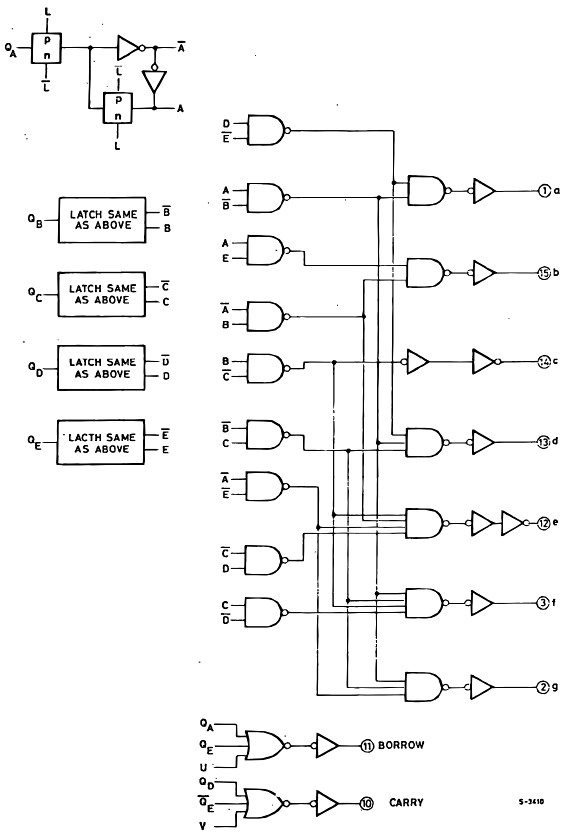
| CLOCK UP* | CLOCK DOWN* | LATCH ENABLE | TOGGLE ENABLE | RESET | COUNTER | DISPLAY |
|---|---|---|---|---|---|---|
| _\|‾ | X | L | L | L | Increments by 1 | Follows Counter |
| X | _\|‾ | L | L | L | Decrements by 1 | Follows Counter |
| ‾\|_ | ‾\|_ | X | X | L | No Change | No Change |
| X | X | X | X | H | Goes to 00000 | Follow Counter (Display = 0) |
| X | X | X | H | L | Inhibited | Remains Fixed |
| _\|‾ | X | H | L | L | Increments by 1 | Remains Fixed |
| X | _\|‾ | H | L | L | Decrements by 1 | Remains Fixed |

X : Don't Care
* : Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting

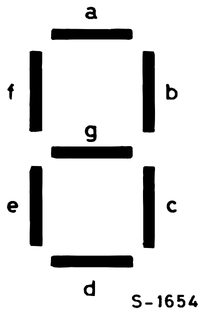
## LOGIC DIAGRAM

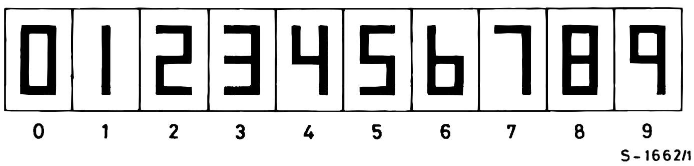


## LOGIC DIAGRAM




## DISPLAY SEGMENTS



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | -0.5 to +22 | V |
| $V_I$ | DC Input Voltage | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current | ± 10 | mA |
| $P_D$ | Power Dissipation per Package | 200 | mW |
| | Power Dissipation per Output Transistor | 100 | mW |
| $T_{op}$ | Operating Temperature | -55 to +125 | °C |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to $V_{SS}$ pin voltage.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3 to 20 | V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature | -55 to 125 | °C |

## DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $V_O$ (V) | $\|I_O\|$ (µA) | $V_{DD}$ (V) | $T_A = 25°C$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | 0/5 | | | 5 | | 0.04 | 5 | | 150 | | 150 | µA |
| | | 0/10 | | | 10 | | 0.04 | 10 | | 300 | | 300 | |
| | | 0/15 | | | 15 | | 0.04 | 20 | | 600 | | 600 | |
| | | 0/20 | | | 20 | | 0.08 | 100 | | 3000 | | 3000 | |
| $V_{OH}$ | High Level Output Voltage | 0/5 | | <1 | 5 | 4.95 | | | 4.95 | | 4.95 | | V |
| | | 0/10 | | <1 | 10 | 9.95 | | | 9.95 | | 9.95 | | |
| | | 0/15 | | <1 | 15 | 14.95 | | | 14.95 | | 14.95 | | |
| $V_{OL}$ | Low Level Output Voltage | 5/0 | | <1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | 10/0 | | <1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | 15/0 | | <1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | High Level Input Voltage | | 0.5/4.5 | <1 | 5 | 3.5 | | | 3.5 | | 3.5 | | V |
| | | | 1/9 | <1 | 10 | 7 | | | 7 | | 7 | | |
| | | | 1.5/13.5 | <1 | 15 | 11 | | | 11 | | 11 | | |
| $V_{IL}$ | Low Level Input Voltage | | 4.5/0.5 | <1 | 5 | | | 1.5 | | 1.5 | | 1.5 | V |
| | | | 9/1 | <1 | 10 | | | 3 | | 3 | | 3 | |
| | | | 13.5/1.5 | <1 | 15 | | | 4 | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | 0/5 | 2.5 | <1 | 5 | -1.36 | -3.2 | | -1.1 | | -1.1 | | mA |
| | | 0/5 | 4.6 | <1 | 5 | -0.44 | -1 | | -0.36 | | -0.36 | | |
| | | 0/10 | 9.5 | <1 | 10 | -1.1 | -2.6 | | -0.9 | | -0.9 | | |
| | | 0/15 | 13.5 | <1 | 15 | -3.0 | -6.8 | | -2.4 | | -2.4 | | |
| $I_{OL}$ | Output Sink Current Q | 0/5 | 0.4 | <1 | 5 | 1.74 | 4 | | 1.43 | | 1.43 | | mA |
| | | 0/10 | 0.5 | <1 | 10 | 4.42 | 10.4 | | 3.74 | | 3.74 | | |
| | | 0/15 | 1.5 | <1 | 15 | 11.56 | 27.2 | | 9.52 | | 9.52 | | |
| $I_{OL}$ | Output Sink Current | 0/5 | 0.4 | <1 | 5 | 0.44 | 1 | | 0.36 | | 0.36 | | mA |
| | | 0/10 | 0.5 | <1 | 10 | 1.1 | 2.6 | | 0.9 | | 0.9 | | |
| | | 0/15 | 1.5 | <1 | 15 | 3.0 | 6.8 | | 2.4 | | 2.4 | | |
| $I_I$ | Input Leakage Current | 0/18 | Any Input | | 18 | | $\pm 10^{-5}$ | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | 3-State Output Leakage Current | 0/18 | Any Input | | 18 | | $\pm 10^{-4}$ | ±0.4 | | ±12 | | ±12 | µA |
| $C_I$ | Input Capacitance | | Any Input | | | | 5 | 7.5 | | | | | pF |

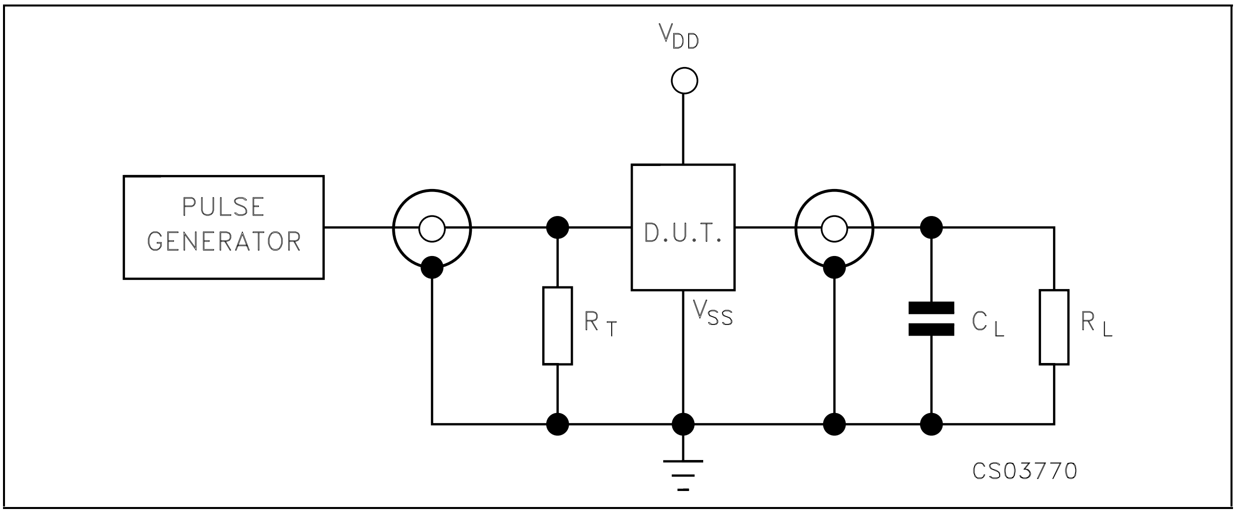
The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}$=5V, 2V min. with $V_{DD}$=10V, 2.5V min. with $V_{DD}$=15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C, $C_L$ = 50pF, $R_L$ = 200KΩ, $t_r = t_f$ = 20 ns)

| Symbol | Parameter | Test Condition | | Value (*) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | | Min. | Typ. | Max. | |
| **CLOCK UP/CLOCK DOWN** | | | | | | | |
| $t_W$ | Pulse Width | 5 | | | 85 | | ns |
| | | 10 | | | 35 | | |
| | | 15 | | | 15 | | |
| $f_{CL}$ | Maximum Frequency | 5 | | | 2.5 | | MHz |
| | | 10 | | | 5 | | |
| | | 15 | | | 8 | | |
| $t_{WC}$ | Carry Pulse Width | 5 | | | 225 | | ns |
| | | 10 | | | 100 | | |
| | | 15 | | | 70 | | |
| $t_{WB}$ | Borrow Pulse Width | 5 | | | 260 | | ns |
| | | 10 | | | 110 | | |
| | | 15 | | | 80 | | |
| **RESET** | | | | | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time Reset to Clock | 5 | | | 750 | | ns |
| | | 10 | | | 285 | | |
| | | 15 | | | 200 | | |
| | Delay from Reset to First Allowable Clock | 5 | | | 300 | | ns |
| | | 10 | | | 125 | | |
| | | 15 | | | 75 | | |
| $t_W$ | Pulse Width | 5 | | | 150 | | ns |
| | | 10 | | | 60 | | |
| | | 15 | | | 40 | | |

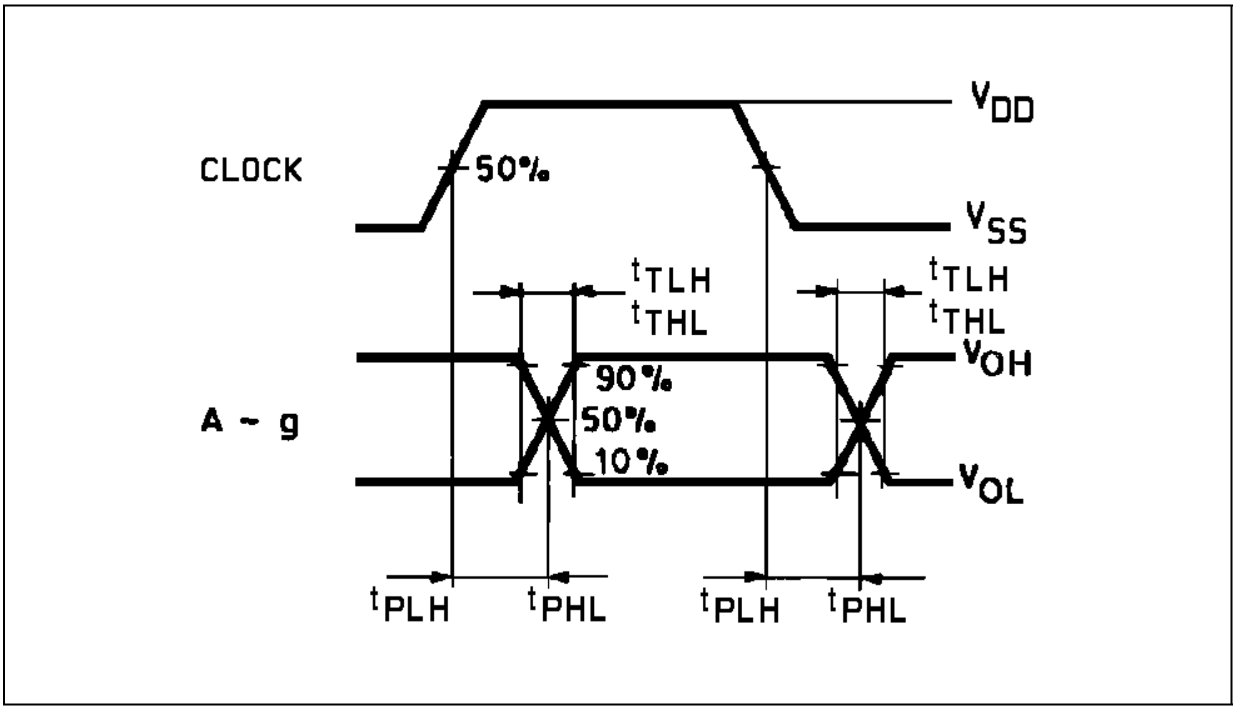
(*) Typical temperature coefficient for all $V_{DD}$ value is 0.3 %/°C.
NOTE : Measured at the point of 10% change in output load of 50pF, $R_L$ = 1KΩ to $V_{DD}$ for $t_{PZL}$, $t_{PLZ}$ and $R_L$ = 1KΩ to $V_{SS}$ for $t_{PHZ}$

**TEST CIRCUIT**



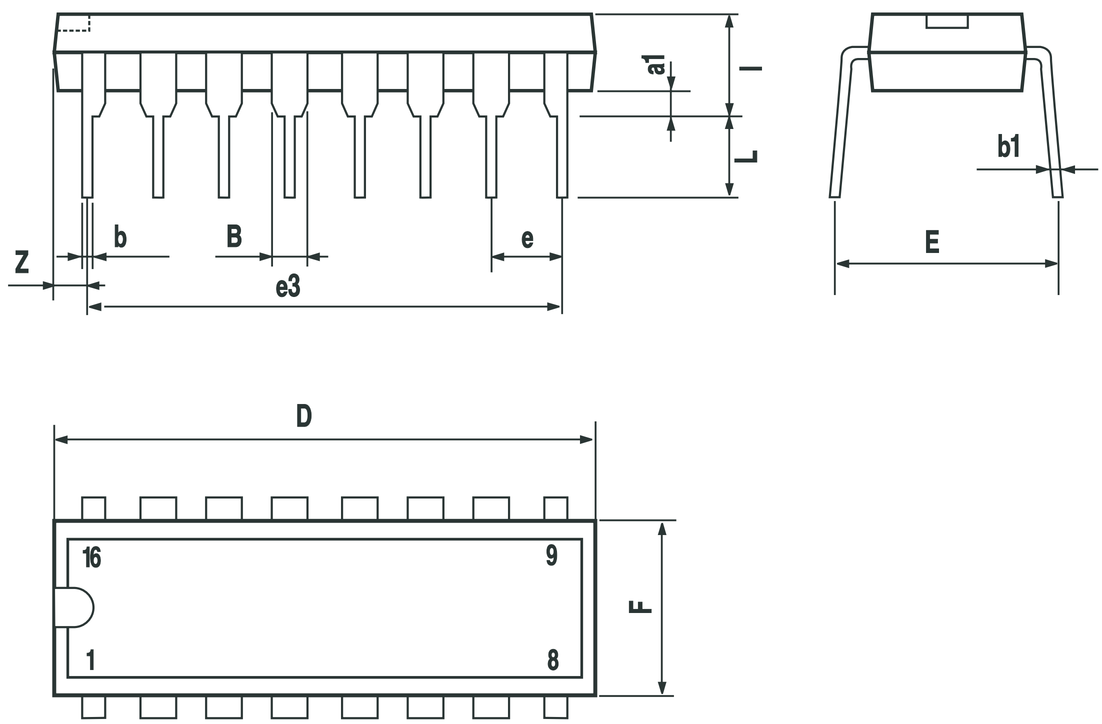

$C_L$ = 50pF or equivalent (includes jig and probe capacitance)
$R_L$ = 200KΩ
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)

**WAVEFORM : PROPAGATION DELAY TIMES** (f=1MHz; 50% duty cycle)



## Plastic DIP-16 (0.25) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |




P001C