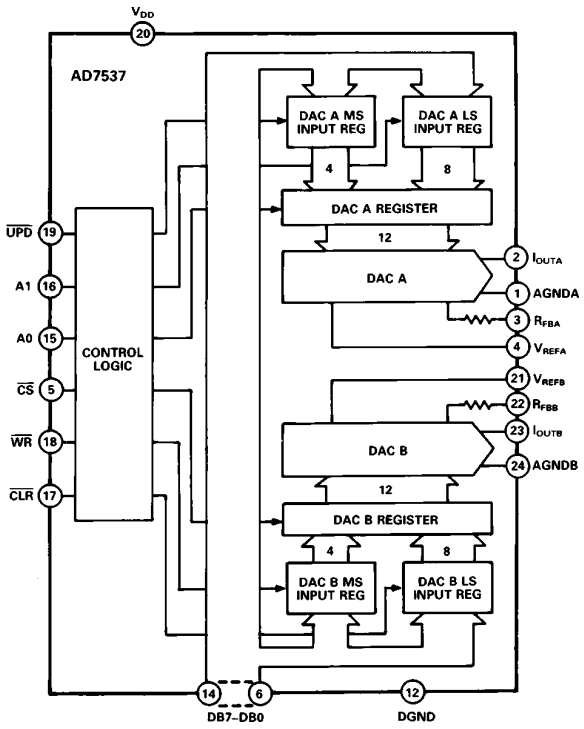
LC²MOS (8+4) Loading Dual 12-Bit DAC

AD7537

FEATURES
Two 12-Bit DACs in One Package
DAC Ladder Resistance Matching: 0.5%
Space Saving Skinny DIP and Surface Mount Packages
4-Quadrant Multiplication
Low Gain Error (1 LSB max Over Temperature)
Byte Loading Structure
Fast Interface Timing

APPLICATIONS
Automatic Test Equipment
Programmable Filters
Audio Applications
Synchro Applications
Process Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7537 contains two 12-bit current output DACs on one monolithic chip. A separate reference input is provided for each DAC. The dual DAC saves valuable board space, and the monolithic construction ensures excellent thermal tracking. Both DACs are guaranteed 12-bit monotonic over the full temperature range.

The AD7537 has a 2-byte (8 LSBs, 4 MSBs) loading structure. It is designed for right-justified data format. The control signals for register loading are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{UPD}$. Data is loaded to the input registers when $\overline{CS}$ and $\overline{WR}$ are low. To transfer this data to the DAC registers, $\overline{UPD}$ must be taken low with $\overline{WR}$.

Added features on the AD7537 include an asynchronous $\overline{CLR}$ line which is very useful in calibration routines. When this is taken low, all registers are cleared. The double buffering of the data inputs allows simultaneous update of both DACs. Also, each DAC has a separate AGND line. This increases the device versatility; for instance one DAC may be operated with AGND biased while the other is connected in the standard configuration.

The AD7537 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC and 5 V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching:
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size:
   The AD7537 is packaged in small 24-pin 0.3" DIPs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance:
   The device operates on a +12 V to +15 V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

REV. 0

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AD7537–SPECIFICATIONS

(V_{DD} = +12 V to +15 V, ±10%, V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = AGND = 0 V, I_{OUTB} = AGNDB = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1s.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1 ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14 kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB}								
Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (lnput High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IIL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	µA max	V_{IN} = V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	±10	±10	µA max	
C_{IN} (lnput Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12 V to +15 V; V_{REFA} = V_{REFB} = +10 V; I_{OUTA} = AGNDA = 0 V, I_{OUTB} = AGNDB = 0 V. Output Amplifiers are AD644 except where noted.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5		µs max	To 0.01% of full-scale range. I_{OUT} load = 100 Ω, C_{EXT} = 13 pF. DAC output measured from falling edge of $\overline{WR}$. Typical Value of Settling Time is 0.8 µs.
Digital-to-Analog Glitch lmpulse	7		nV-s typ	Measured with V_{REFA} = V_{REFB} = 0 V. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	–70	–65	dB max	V_{REFA}, V_{REFB} = 20 V p-p 10 kHz sine wave.
V_{REFB} to I_{OUTB}	–70	–65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max – V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0s
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1s
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	–84		dB typ	V_{REFA} = 20 V p-p 10 kHz sine wave, V_{REFB} = 0 V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	–84		dB typ	V_{REFB} = 20 V p-p 10 kHz sine wave, V_{REFA} = 0 V. Both DACs loaded with all 1s.
Digital Crosstalk	7		nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF.
Output Noise Voltage Density (10 Hz–100 kHz)	25		nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10 Hz–100 kHz.
Total Harmonic Distortion	–82		dB typ	V_{IN} = 6 V rms, 1 kHz. Both DACs loaded with all 1s.

NOTES

[1]Temperature range as follows: J, K, L Versions: –40°C to +85°C; A, B, C Versions: –40°C to +85°C; S, T, U Versions: –55°C to +125°C

[2]Sample tested at +25°C to ensure compliance.

[3]Functional at V_{DD} = 5 V, with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +10.8 V to +16.5 V, V_{REFA} = V_{REFB} = +10 V; I_{OUTA} = AGNDA = 0 V, I_{OUTB} = AGNDB = 0 V.)

Parameter	Limit at T_A = +25°C	Limit at T_A = –40°C to +85°C	Limit at T_A = +55°C to +125°C	Units	Test Conditions/Comments
t_1	15	15	30	ns min	Address Valid to Write Setup Time
t_2	15	15	25	ns min	Address Valid to Write Hold Time
t_3	60	80	80	ns min	Data Setup Time
t_4	25	25	25	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	80	80	100	ns min	Write Pulse Width
t_8	80	80	100	ns min	Clear Pulse Width

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

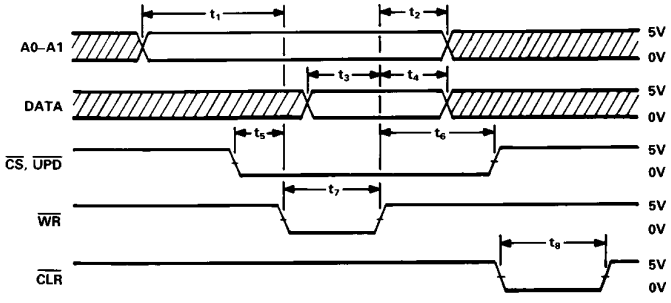
(T_A = +25°C unless otherwise stated)

V_{DD} to DGND ..... –0.3 V, +17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB ..... ±25 V
V_{RFBA}, V_{RFBB} to AGNDA, AGNDB ..... ±25 V
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} +0.3 V
I_{OUTA}, I_{OUTB} to DGND ..... –0.3 V, V_{DD} +0.3 V
AGNDA, AGNDB to DGND ..... –0.3 V, V_{DD} +0.3 V
Power Dissipation (Any Package)
To +75°C ..... 450 mW
Derates Above +75°C ..... 6 mW/°C
Operating Temperature Range
Commercial Plastic (J, K, L Versions) .... –40°C to +85°C
Industrial Hermetic (A, B, C Versions) ... –40°C to +85°C
Extended Hermetic (S, T, U Versions) .. –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7537 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_r = t_f = 20$ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. Timing Diagram

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7537JN	–40°C to +85°C	±1 LSB	±6 LSB	N-24
AD7537KN	–40°C to +85°C	±1/2 LSB	±3 LSB	N-24
AD7537LN	–40°C to +85°C	±1/2 LSB	±1 LSB	N-24
AD7537JP	–40°C to +85°C	±1 LSB	±6 LSB	P-28A
AD7537KP	–40°C to +85°C	±1/2 LSB	±3 LSB	P-28A
AD7537LP	–40°C to +85°C	±1/2 LSB	±1 LSB	P-28A
AD7537AQ	–40°C to +85°C	±1 LSB	±6 LSB	Q-24
AD7537BQ	–40°C to +85°C	±1/2 LSB	±3 LSB	Q-24
AD7537CQ	–40°C to +85°C	±1/2 LSB	±1 LSB	Q-24
AD7537SQ	–55°C to +125°C	±1 LSB	±6 LSB	Q-24
AD7537TQ	–55°C to +125°C	±1/2 LSB	±3 LSB	Q-24
AD7537UQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-24
AD7537SE	–55°C to +125°C	±1 LSB	±6 LSB	E-28A
AD7537TE	–55°C to +125°C	±1/2 LSB	±3 LSB	E-28A
AD7537UE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-28A

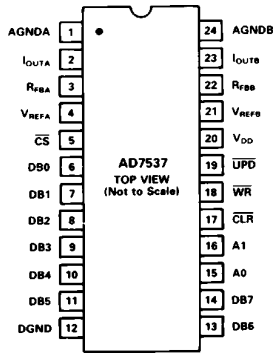
NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.

PIN FUNCTION DESCRIPTION (DIP)

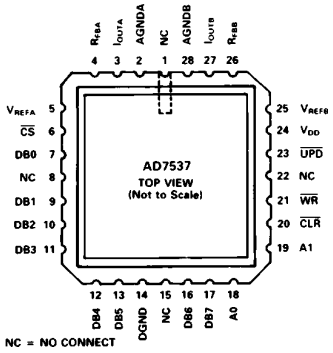
PIN	MNEMONIC	DESCRIPTION
1	AGNDA	Analog Ground for DAC A.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CS}$	Chip Select Input Active low.
6–14	DB0–DB7	Eight data inputs, DB0–DB7.
12	DGND	Digital Ground.
15	A0	Address Line 0.
16	A1	Address Line 1.
17	$\overline{CLR}$	Clear Input. Active low. Clears all registers.
18	$\overline{WR}$	Write Input. Active low.
19	$\overline{UPD}$	Updates DAC Registers from inputs registers.
20	V_{DD}	Power supply input. Nominally +12 V to +15 V, with ±10% tolerance.
21	V_{REFB}	Reference input to DAC B.
22	R_{FBB}	Feedback resistor for DAC B.
23	I_{OUTB}	Current output terminal of DAC B.
24	AGNDB	Analog Ground for DAC B.

PIN CONFIGURATIONS

DIP



LCCC



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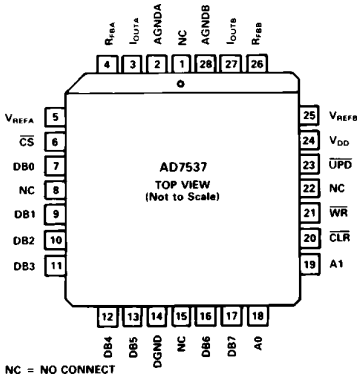


CIRCUIT INFORMATION – D/A SECTION

The AD7537 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGNDA. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op amp (see Figures 4 and 5) to convert the current flowing in I_{OUTA} to a voltage output.

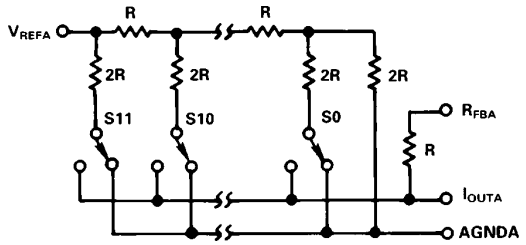


Figure 2. Simplified Circuit Diagram for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7537. A similar equivalent circuit can be drawn for DAC B.

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50 pF to 150 pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_0 is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA.

Table I. AD7537 Truth Table

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)–DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)–DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

NOTES: X = Don't care

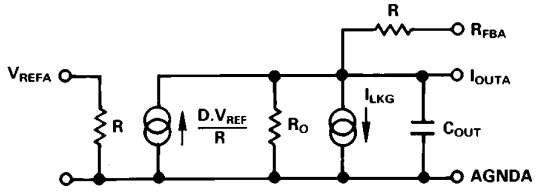


Figure 3. Equivalent Analog Circuit for DAC A

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (AD644, AD712) or separate packages (AD544, AD711, AD OP27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high-speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0 V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7537, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

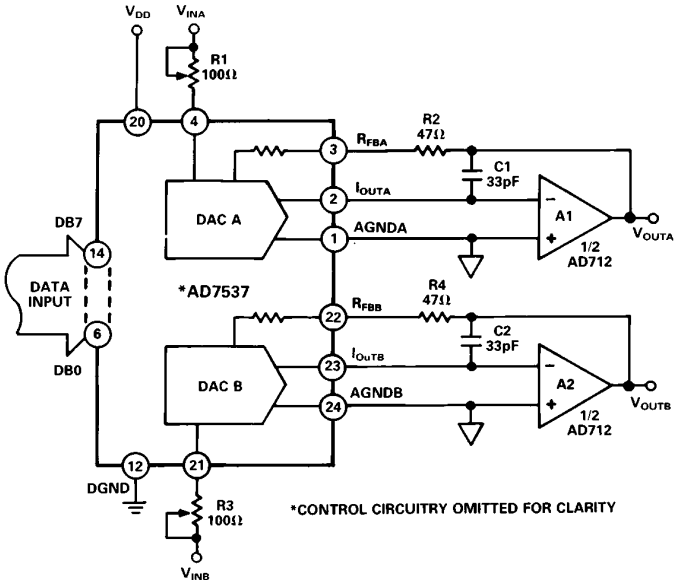


Figure 4. AD7537 Unipolar Binary Operation

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0 V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, 10) varied for V_{OUTA} (V_{OUTB}) = 0 V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 5 is given in Table III.

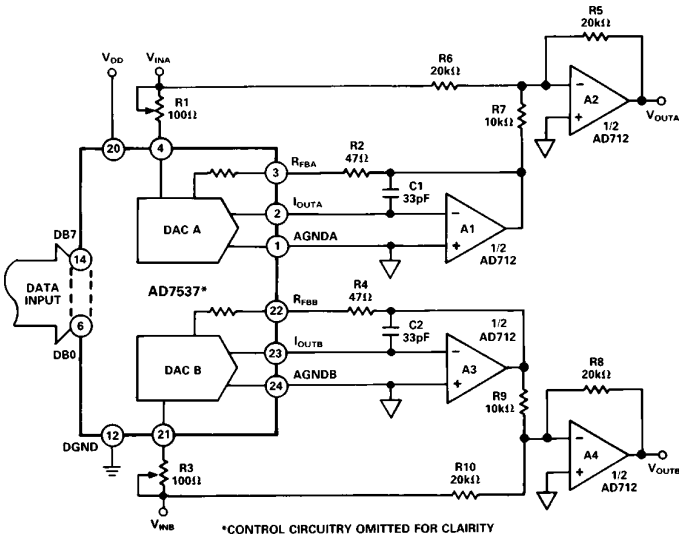


Figure 5. Bipolar Operation (Offset Binary Coding)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$

SEPARATE AGND PINS

The DACs in the AD7537 have separate AGND lines taken to pins AGNDA and AGNDB on the package. This increases the applications versatility of the part. Figure 6 is an example of this. DAC A is connected in standard fashion as a programmable attenuator. AGNDA is at ground potential. DAC B is operating with AGND B biased to +5 V by the AD584. This gives an output range of +5 V to +10 V.

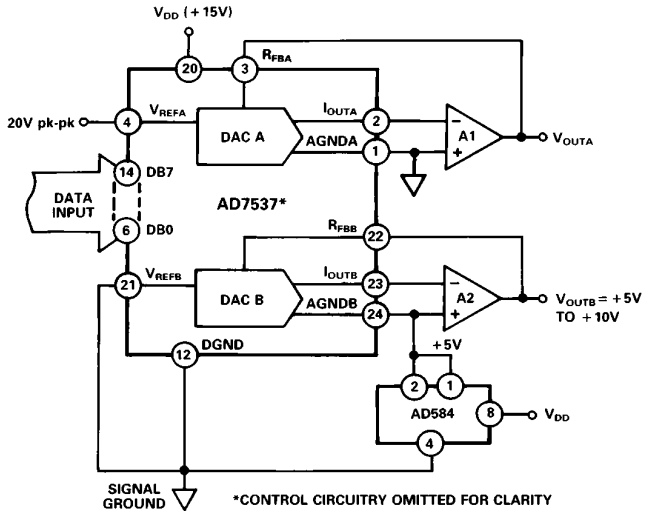


Figure 6. AD7537 DACs Used in Different Modes

PROGRAMMABLE OSCILLATOR

Figure 7 shows a conventional state variable oscillator in which the AD7537 controls the programmable integrators. The frequency of oscillation is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}\times\frac{1}{C1\times C2\times R_{EQ1}\times R_{EQ2}}}$$

where R_{EQ1} and R_{EQ2} are the equivalent resistances of the DACs. The same digital code is loaded into both DACs. If C1 = C2 and R5 = R6, the expression reduces to

$$f = \frac{1}{2\pi}\times\frac{1}{C}\sqrt{\frac{1}{R_{EQ1}\times R_{EQ2}}}$$

Since $R_{EQ} = \frac{2^n \times R_{LAD}}{N}$, ($R_{LAD}$ = DAC ladder resistance).

$$f = \frac{1}{2\pi}\times\frac{1}{C}\sqrt{\frac{(N/2^n)^2}{R_{LAD1}\times R_{LAD2}}}$$

$$= \frac{1}{2\pi}\times\frac{D}{C}\frac{1}{\sqrt{R_{LAD1}\times R_{LAD2}}} \qquad D = \left(\frac{N}{2^n}\right)$$

$$= \frac{1}{2\pi}\times\frac{D}{C\times R_{LAD}\sqrt{m}}$$

where m is the DAC ladder resistance mismatch ratio, typically 1.005.

With the values shown in Figure 7, the output frequency varies from 0 Hz to 1.38 kHz. The amplitude of the output signal at the A3 output is 10 V peak-to-peak and is constant over the entire frequency span.

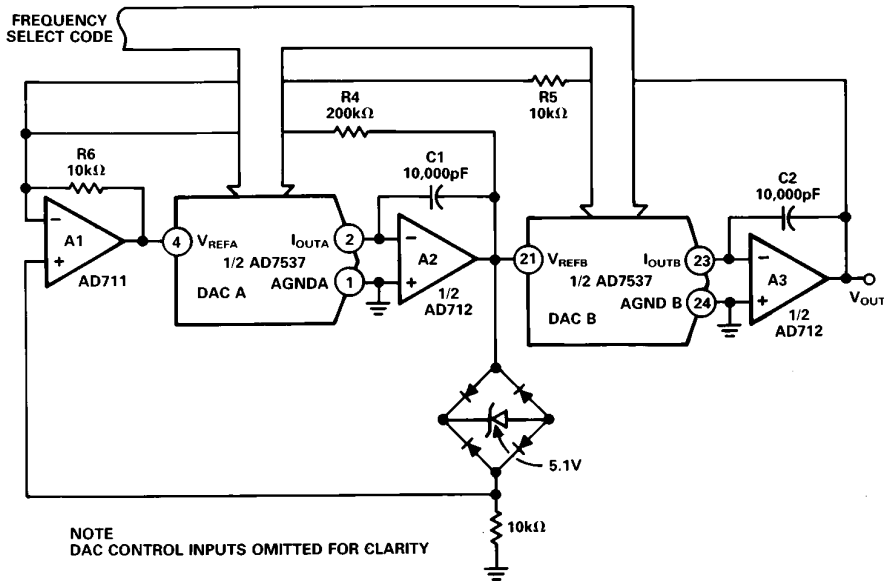


Figure 7. Programmable State Variable Oscillator

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified operation, it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are the AD711C and its dual version, the AD712C. These op amps have a wide bandwidth and high slew rate and are recommended for wide bandwidth ac applications. AD711/AD712 settling time to 0.01% is typically 3 μs.

Temperature Coefficients: The gain temperature coefficient of the AD7537 has a maximum value of 5 ppm/°C and typical value of 1 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.4 LSBs respectively over a 100°C temperature range. When trim resistors R1 (R3) and R2 (R4) are used to adjust full scale range as in Figure 4, the temperature coefficient of R1 (R3) and R2 (R4) should also be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Application Note, Publication Number E630c-5-3/86 available from Analog Devices.

High Frequency Considerations: AD7537 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 and C2 in Figures 4 and 5.

Feedthrough: The dynamic performance of the AD7537 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 4 is shown in Figure 8 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

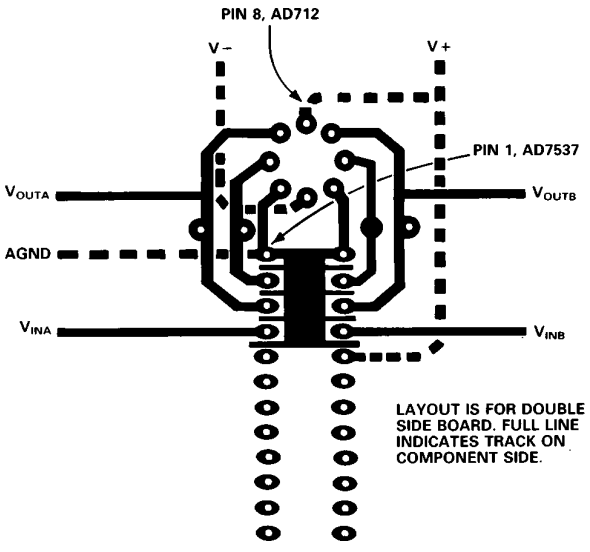


Figure 8. Suggested Layout for AD7537

MICROPROCESSOR INTERFACING

The byte loading structure of the AD7537 makes it very easy to interface the device to any 8-bit microprocessor system. Figures 9 and 10 show two interfaces: one for the MC6809 and the other for the MC68008. Figure 11 shows how an AD7537 system can be easily expanded by tying all the $\overline{UPD}$ lines together and using a single decoder output to control these. This expanded system is shown using a Z80 microprocessor but it is just as easily configured using any other 8-bit microprocessor system. Note how the system shown in Figure 11 produces 4 analog outputs with a minimum amount of hardware.

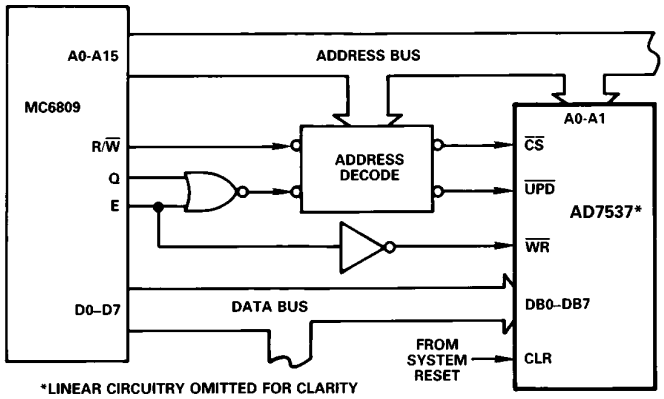


Figure 9. AD7537–MC6809 Interface

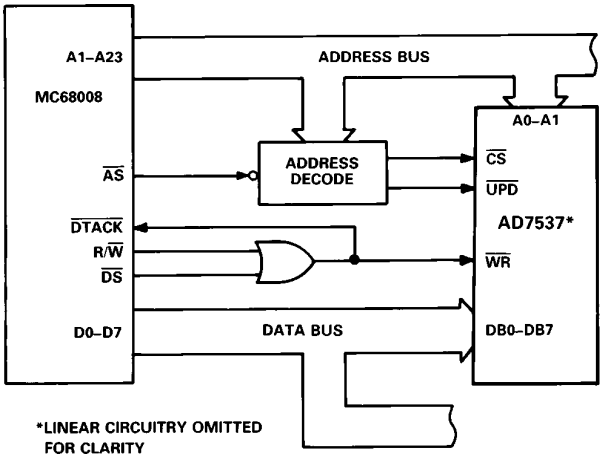


Figure 10. AD7537–MC68008 Interface

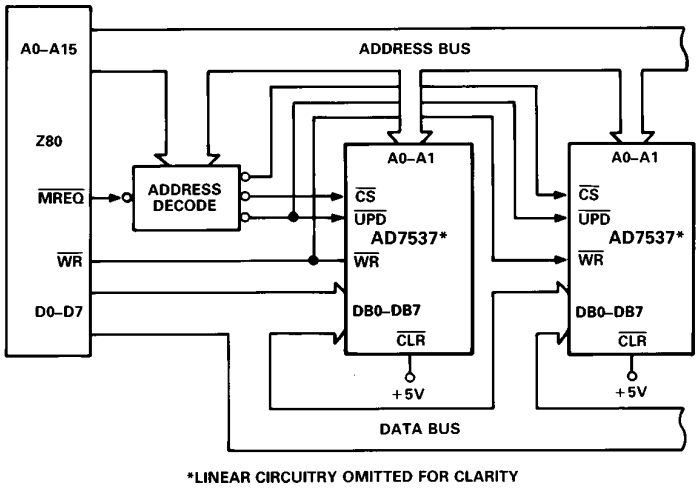
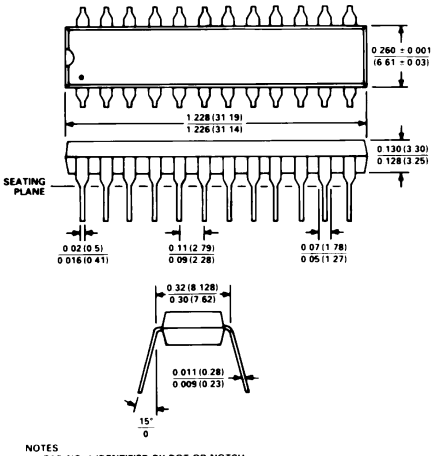


Figure 11. Expanded AD7537 System

OUTLINE DIMENSIONS

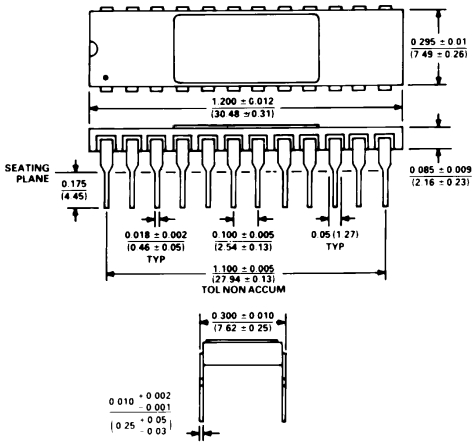
Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



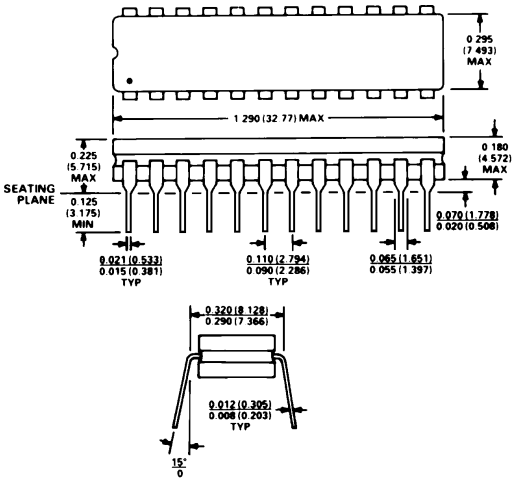
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Ceramic DIP (D-24A)



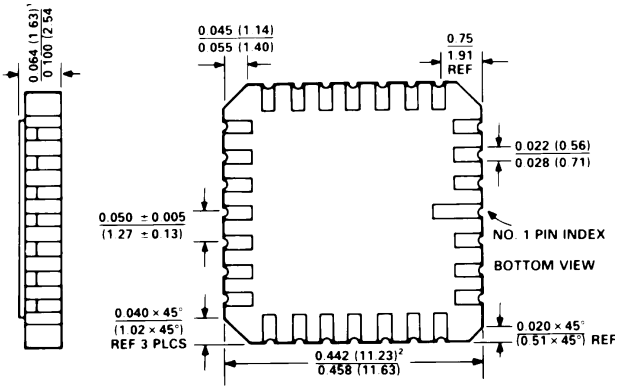
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.
3. METAL LID IS CONNECTED TO DGND.

24-Pin Cerdip (Q-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Terminal Leadless Ceramic Chip Carrier (E-28A)



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-Terminal Plastic Leaded Chip Carrier (P-28A)