UMC

UM6264 Series

8K× 8 CMOS SRAM

Features

- Single +5 volt power supply
- Access times: 70/100/120 ns (max.)
- Current:
  - Standard version: Operating: 90 mA (max.)
    Standby: 2 mA (max.)
  - Low power version: Operating: 90 mA (max.)
    Standby: 100μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Output enable and two chip select inputs for easy application
- Data retention voltage: 2V (min.) for low power version
- Available in 28 pin DIP, SOP, or Skinny DIP packages (See ordering information)

General Description

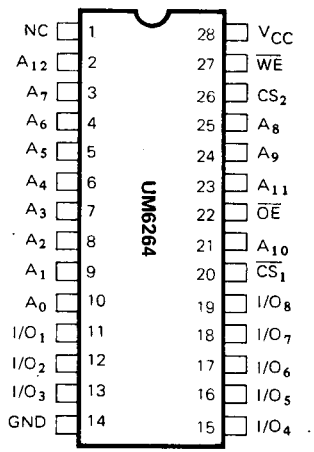
The UM6264 is a high-speed, low-power 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates on a single 5-volt power supply. It is built using UMC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

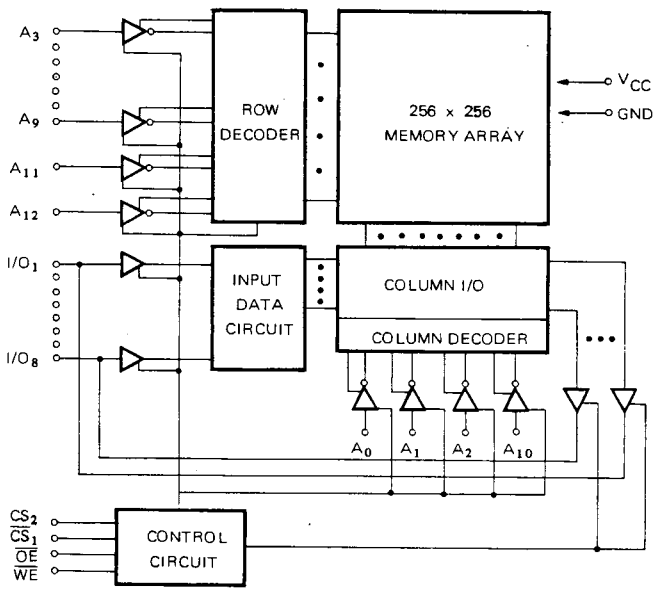
Two chip select inputs are provided for power down and device select, and an output enable input is included for easy interface.

Data retention is guaranteed at a power supply voltage as low as 2V for the low power version.

Pin Configuration



Block Diagram



Pin Description

Designation	Description
$A_0 \sim A_{12}$	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
NC	No Connection
$I/O_1 \sim I/O_8$	Data Input/Output
V_{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC}+ 0.5V	V
V_{IL}	Input Low Voltage	–0.3	0	+0.8	V
C_L	Output Load	–	–	100	pF
TTL	Output Load	–	–	1	–

Absolute Maximum Ratings *

V_{CC} to GND ..... –0.5V to +7.0V
IN, IN/OUT Volt to GND ..... –0.5V to V_{CC} +0.5V
Operating Temperature, T_{opr} ..... 0°C to +70°C
Storage Temperature, T_{stg} ..... –55°C to +125°C
Temperature Under Bias, T_{bias} ..... –10°C to +85°C
Power Dissipation, P_T 1.0W/SOP 0.7W
Soldering temp. & time ..... 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM6264-70/10/12 Min.	UM6264-70/10/12 Max.	UM6264-70L/10L/12L Min.	UM6264-70L/10L/12L Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Leakage Current	–	2	–	2	μA	V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current	–	2	–	2	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}
I_{CC}	Active Power Supply Current	–	90	–	90	mA	$\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} $I_{I/O}$ = 0 mA
I_{CC1}	Dynamic Operating Current	–	90	–	90	mA	Min. Cycle, Duty = 100% $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	–	5	–	3	mA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL}
I_{SB1}		–	2	–	0.1	mA	$\overline{CS_1}$ ≥ V_{CC} – 0.2V, CS_2 ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V
I_{SB2}		–	2	–	0.1	mA	$\overline{CS_1}$ ≤ 0.2V, CS_2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	–	0.4	–	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4	–	2.4	–	V	I_{OH} = –1.0 mA

Truth Table

Mode	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O Operation	V_{CC} Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disabled	L	H	H	H	High Z	I_{CC}, I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: X : H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* This parameter is sampled and not 100% tested

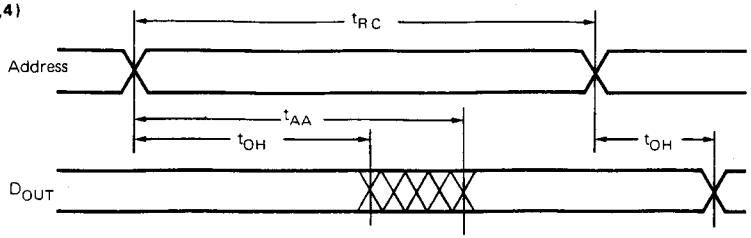
AC Characteristics (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter		UM6264-70/70L Min.	UM6264-70/70L Max.	UM6264-10/10L Min.	UM6264-10/10L Max.	UM6264-12/12L Min.	UM6264-12/12L Max.	Unit
Read Cycle									
t_{RC}	Read Cycle Time		70	–	100	–	120	–	ns
t_{AA}	Address Access Time		–	70	–	100	–	120	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS_1}$	–	70	–	100	–	120	ns
t_{ACS2}		CS_2	–	70	–	100	–	120	ns
t_{OE}	Output Enable to Output Valid		–	35	–	50	–	60	ns
t_{CLZ1}	Chip Selection to Output in Low Z	$\overline{CS_1}$	10	–	10	–	10	–	ns
t_{CLZ2}		CS_2	10	–	10	–	10	–	ns
t_{OLZ}	Output Enable to Output in Low Z		5	–	5	–	5	–	ns
t_{CHZ1}	Chip Deselection to Output in High Z	$\overline{CS_1}$	0	35	0	35	0	40	ns
t_{CHZ2}		CS_2	0	35	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High Z		0	30	0	35	0	40	ns
t_{OH}	Output Hold from Address Change		10	–	10	–	10	–	ns
Write Cycle									
t_{WC}	Write Cycle Time		70	–	100	–	120	–	ns
t_{CW}	Chip Selection to End of Write		60	–	80	–	85	–	ns
t_{AS}	Address Set-up Time		0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write		60	–	80	–	85	–	ns
t_{WP}	Write Pulse Width		50	–	60	–	70	–	ns
t_{WR}	Write Recovery Time		0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z		0	30	0	35	0	40	ns
t_{DW}	Data to Write Time Overlap		30	–	40	–	50	–	ns
t_{DH}	Data Hold from Write Time		0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High Z		0	30	0	35	0	40	ns
t_{OW}	Output Active from End of Write		5	–	10	–	10	–	ns

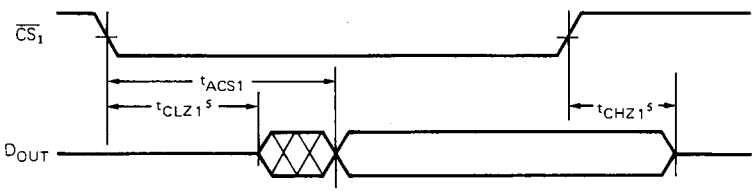
Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms (Continued)

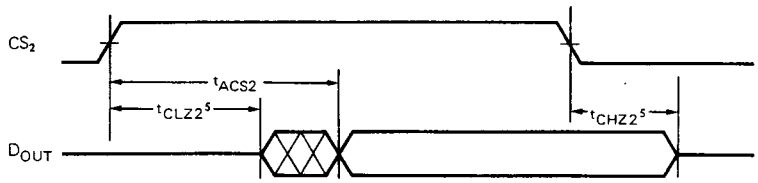
Read Cycle 1 (1,2,4)



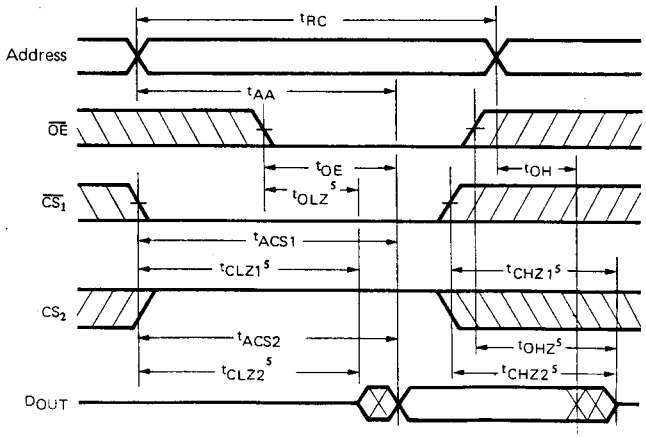
Read Cycle 2 (1,3,4,6)



Read Cycle 3 (1,4,7,8)



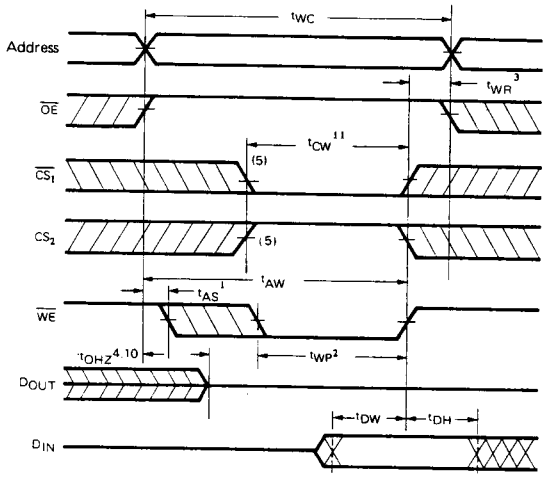
Read Cycle 4 (1)



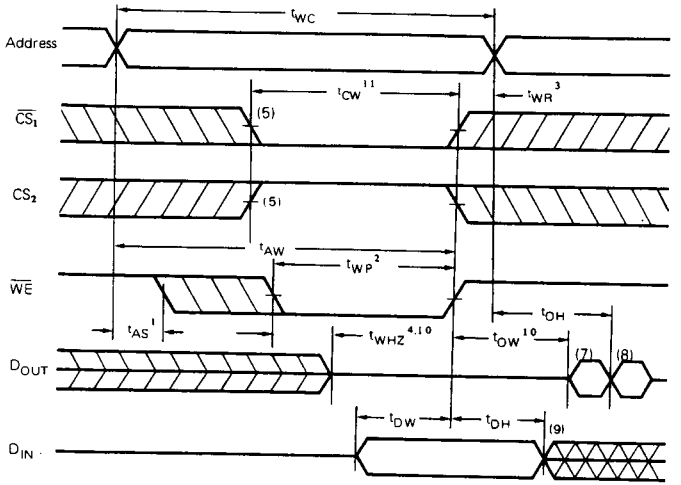
Notes: 1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected $\overline{CS_1} = V_{IL}$ and $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.
8. Address valid prior to or coincident with CS_2 transition high.

Timing Waveforms (Continued)

Write Cycle 1



Write Cycle 2 (6)



Notes:
1. t_{AS} is measured from the address valid to the beginning of write.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occur simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to I/O pins.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{cw} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

AC Test Conditions

For Access Time: 70ns

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 2, 3

For Access Times: 100/120 ns

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 3

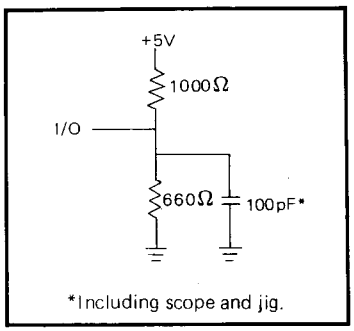


Figure 1. Output Load

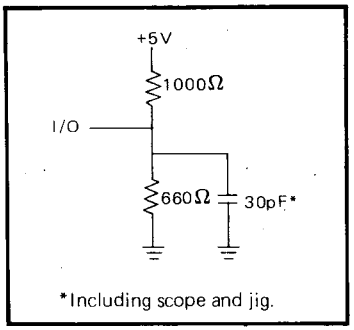


Figure 2. Output Load

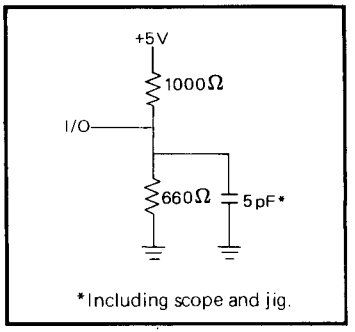


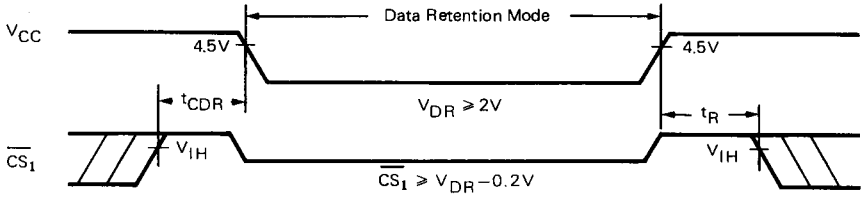
Figure 3. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to +70°C; L version only)

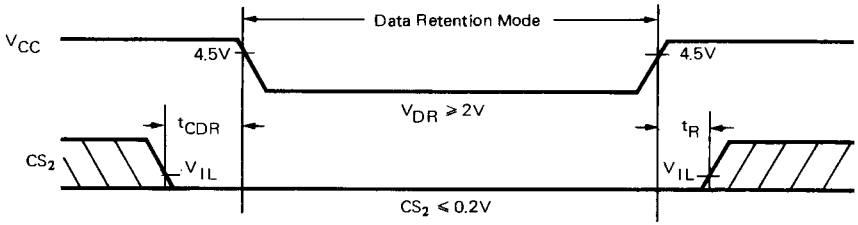
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DR_1}	V_{CC} for Data Retention	2.0	5.5	V	$\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$
V_{DR2}		2.0	5.5	V	$CS_2 \leq 0.2V$
I_{CCDR_1}	Data Retention Current	–	50	μA	V_{CC} = 3.0V, $\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
I_{CCDR_2}		–	50	μA	V_{CC} = 3.0V, $CS_2 \leq 0.2V$, $\overline{CS_1} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	–	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}*	–	ns	

*t_{RC} = Read Cycle Time

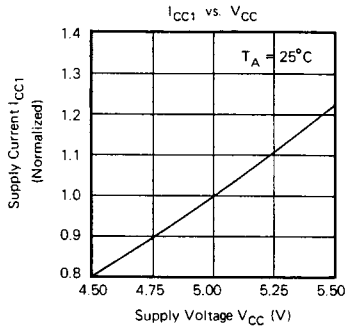
Low V_{CC} Data Retention Waveform (1) ($\overline{CS_1}$ Controlled)

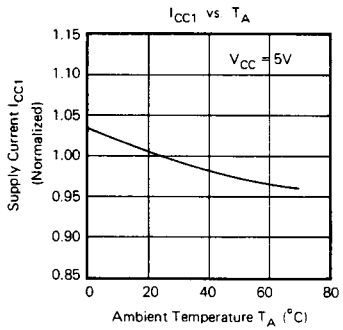


Low V_{CC} Data Retention Waveform (2) (CS_2 Controlled)

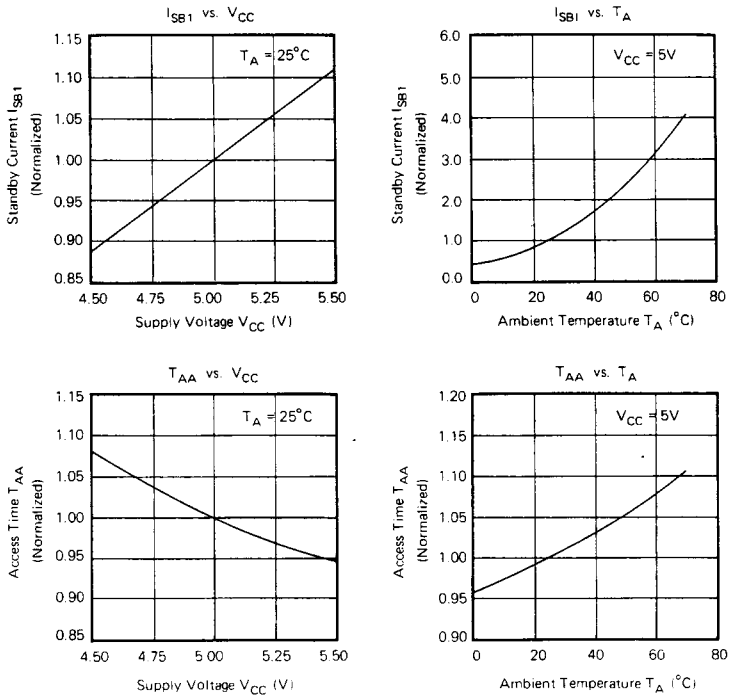


Characteristic Curves





Characteristic Curves (Continued)



Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM6264-70	70	90	2	28L DIP
UM6264-70L		90	0.1	28L DIP
UM6264M-70		90	2	28L SOP
UM6264M-70L		90	0.1	28L SOP
UM6264K-70		90	2	28L Skinny
UM6264K-70L		90	0.1	28L Skinny
UM6264-10	100	90	2	28L DIP
UM6264-10L		90	0.1	28L DIP
UM6264M-10		90	2	28L SOP
UM6264M-10L		90	0.1	28L SOP
UM6264K-10		90	2	28L Skinny
UM6264K-10L		90	0.1	28L Skinny
UM6264-12	120	90	2	28L DIP
UM6264-12L		90	0.1	28L DIP
UM6264M-12		90	2	28L SOP
UM6264M-12L		90	0.1	28L SOP
UM6264K-12		90	2	28L Skinny
UM6264K-12L		90	0.1	28L Skinny