

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4086B

### gates

### 4-wide 2-input AND-OR-invert gate

Product specification  
File under Integrated Circuits, IC04

January 1995

# 4-wide 2-input AND-OR-invert gate

# HEF4086B gates

### DESCRIPTION

The HEF4086B is a 4-wide 2-input AND-OR-invert (AOI) gate with two additional inputs ( $I_8$  or  $\bar{I}_9$ ) which can be used as either expander or inhibit inputs by connecting them to any standard LOCMOS output. A HIGH on  $I_8$  or a LOW on  $\bar{I}_9$  forces the output (O) LOW independent of the other eight inputs ( $I_0$  to  $I_7$ ). The output (O) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

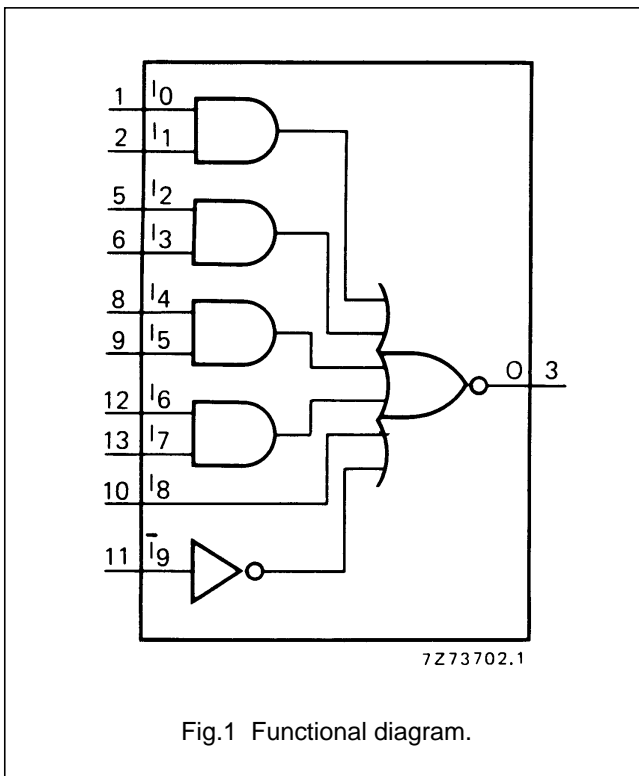


Fig.1 Functional diagram.

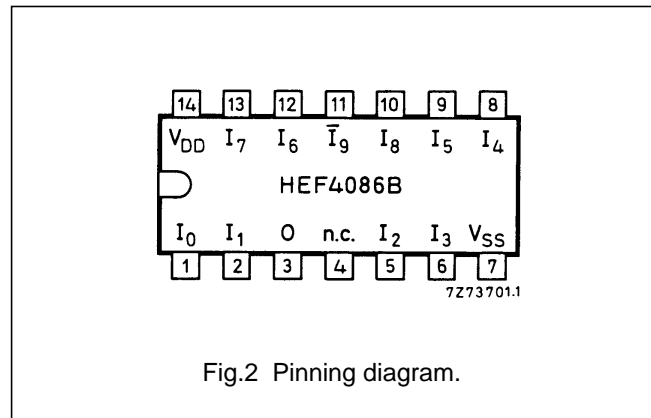


Fig.2 Pinning diagram.

- HEF4086BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4086BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4086BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

### PINNING

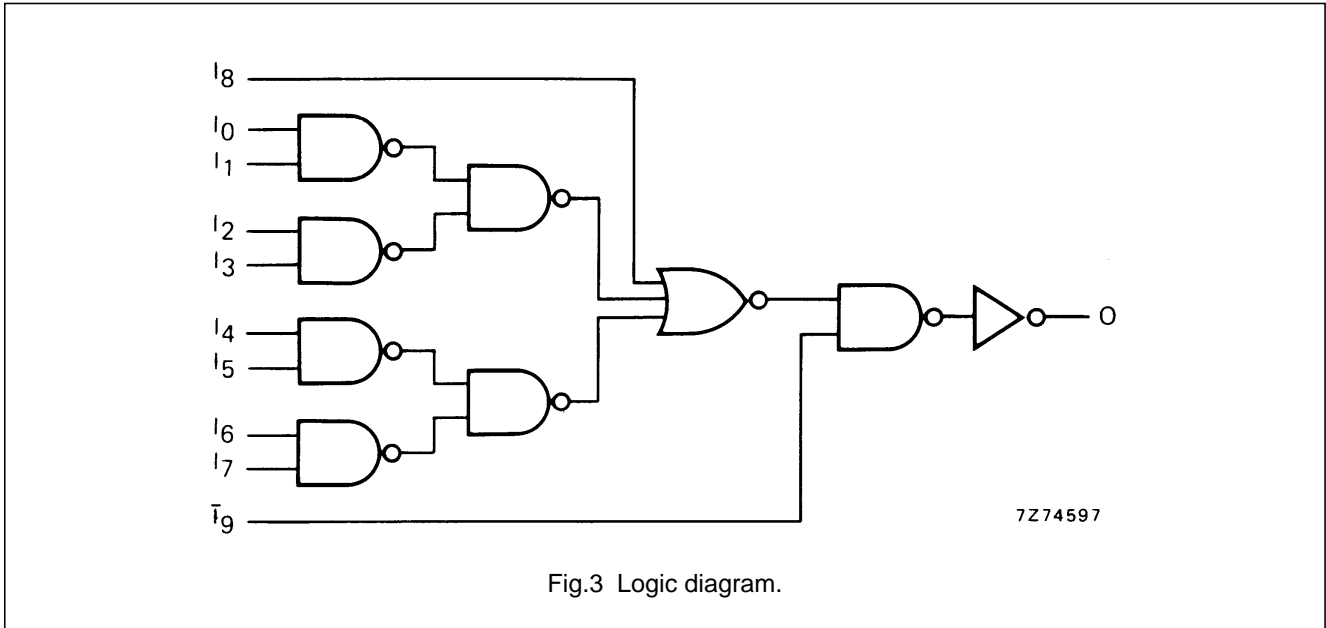
- $I_0$  to  $I_8$  gate inputs
- $\bar{I}_9$  gate input (active LOW)
- O output (active LOW)

### FAMILY DATA, $I_{DD}$ LIMITS category GATES

See Family Specifications

4-wide 2-input AND-OR-invert gate

HEF4086B  
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**LOGIC EQUATION**

$$O = \overline{I_0 \cdot I_1 + I_2 \cdot I_3 + I_4 \cdot I_5 + I_6 \cdot I_7 + I_8 + I_9}$$

## 4-wide 2-input AND-OR-invert gate

HEF4086B  
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	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays	$I_0$ to $I_7 \rightarrow O$ HIGH to LOW	$t_{PHL}$	90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$	
			30	65	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$	
			20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	$t_{PLH}$	80	155	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$	
			30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$	
			20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	$I_8 \rightarrow O$	HIGH to LOW	$t_{PHL}$	70	140	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
				25	55	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
				20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
		LOW to HIGH	$t_{PLH}$	55	115	ns	$28\text{ ns} + (0,55\text{ ns/pF}) C_L$
				20	40	ns	$9\text{ ns} + (0,23\text{ ns/pF}) C_L$
				15	25	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\bar{I}_9 \rightarrow O$	HIGH to LOW	$t_{PHL}$	55	105	ns	$28\text{ ns} + (0,55\text{ ns/pF}) C_L$	
			20	45	ns	$9\text{ ns} + (0,23\text{ ns/pF}) C_L$	
			15	30	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	$t_{PLH}$	45	90	ns	$18\text{ ns} + (0,55\text{ ns/pF}) C_L$	
			15	35	ns	$4\text{ ns} + (0,23\text{ ns/pF}) C_L$	
			10	25	ns	$2\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times	HIGH to LOW	$t_{THL}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	$t_{TLH}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$525 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$2600 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$7300 f_i + \sum (f_o C_L) \times V_{DD}^2$	

4-wide 2-input AND-OR-invert gate

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APPLICATION INFORMATION

Figure 4 shows two HEF4086B ICs connected to obtain an 8-wide 2-input AOI function. The output (O<sub>A</sub>) of the first IC is fed directly into the  $\bar{I}_{9B}$  gate input of the second IC. Similarly, any NAND gate output can be fed directly into the  $\bar{I}_9$  gate input to obtain a 5-wide AOI function. In addition, any AND gate output can be fed directly into the I<sub>8</sub> gate input with the same result.

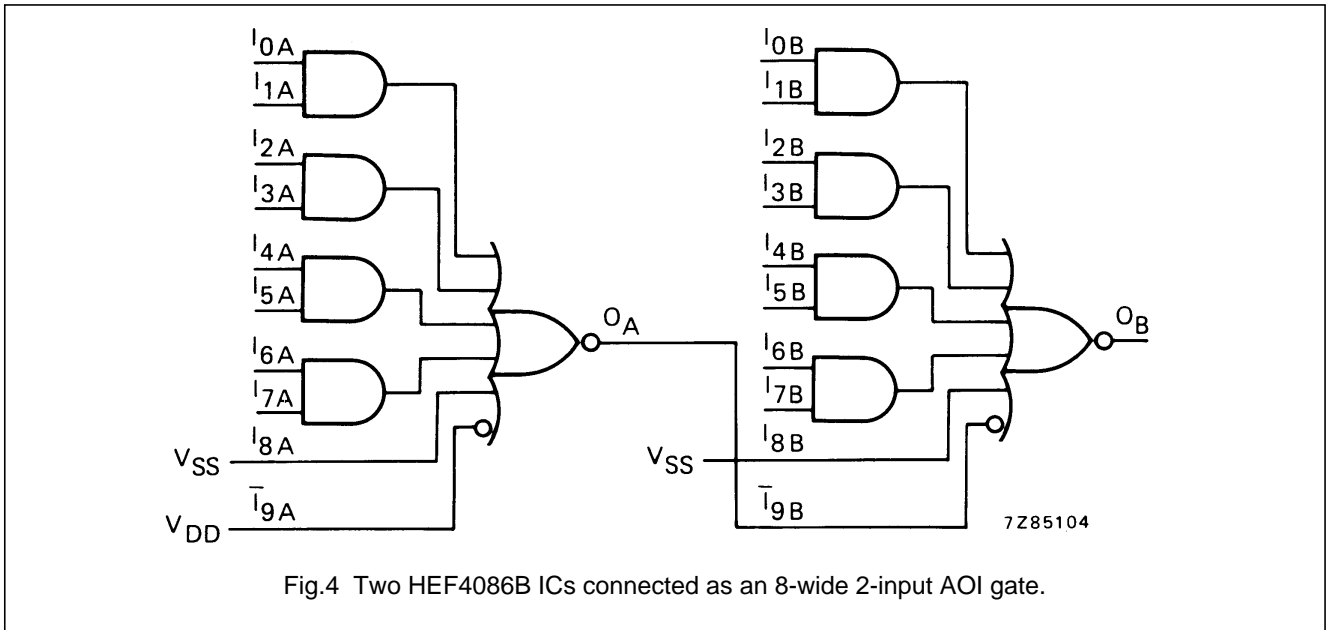


Fig.4 Two HEF4086B ICs connected as an 8-wide 2-input AOI gate.

Logic equation for Fig.4:

$$O_B = \overline{I_{0A} \cdot I_{1A} + I_{2A} \cdot I_{3A} + I_{4A} \cdot I_{5A} + I_{6A} \cdot I_{7A} + I_{0B} \cdot I_{1B} + I_{2B} \cdot I_{3B} + I_{4B} \cdot I_{5B} + I_{6B} \cdot I_{7B}}$$