

# DALLAS

SEMICONDUCTOR

## DS1202, DS1202S

### Serial Timekeeping Chip

#### FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 24 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0–5.5 volt full operation
- Uses less than 300 nA at 2 volts
- Single-byte or multiple-byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL-compatible ( $V_{CC} = 5V$ )
- Optional industrial temperature range  $-40^{\circ}C$  to  $+85^{\circ}C$  (IND)

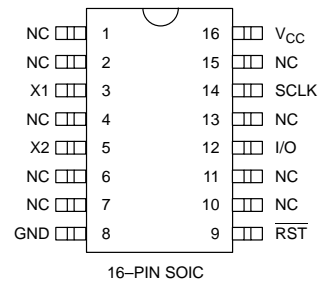
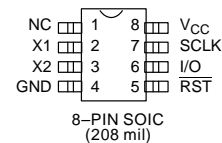
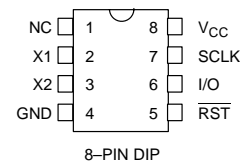
#### ORDERING INFORMATION

DS1202	8-pin DIP
DS1202S	16-pin SOIC
DS1202S-8	8-pin SOIC
DS1202N	8-pin DIP (IND)
DS1202SN	16-pin SOIC (IND)
DS1202SN-8	8-pin SOIC (IND)

#### DESCRIPTION

The DS1202 Serial Timekeeping Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the

#### PIN ASSIGNMENT



#### PIN DESCRIPTION

NC	– No Connection
X1, X2	– 32.768 KHz Crystal Input
GND	– Ground
$\overline{RST}$	– Reset
I/O	– Data Input/Output
SCLK	– Serial Clock
$V_{CC}$	– Power Supply Pin

DS1202 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1)  $\overline{RST}$  (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.



### RESET AND CLOCK CONTROL

All data transfers are initiated by driving the  $\overline{\text{RST}}$  input high. The  $\overline{\text{RST}}$  input serves two functions. First,  $\overline{\text{RST}}$  turns on the control logic which allows access to the shift register for the address/command sequence. Second, the  $\overline{\text{RST}}$  signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. All data transfer terminates if the  $\overline{\text{RST}}$  input is low and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

### DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0. Due to the inherent nature of the logic state machine, writing times containing an absolute value of "59" seconds should be avoided.

### DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as  $\overline{\text{RST}}$  remains high. This operation permits continuous burst mode read capability. Data is output starting with bit 0.

### BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specified clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM registers. When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred.

However, when writing to RAM in burst mode it is not necessary to write all 24 bytes for the data to transfer.

Each byte that is written to will be transferred to RAM regardless of whether all 24 bytes are written or not.

### CLOCK/CALENDAR

The clock/calendar is contained in eight write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

### CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1202 is placed into a low-power standby mode with a current drain of not more than 100 nanoamps. When this bit is written to logic 0, the clock will start.

### AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

### WRITE PROTECT BIT

Bit 7 of the control register is the write protect bit. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

### CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

### RAM

The static RAM is 24 x 8 bytes addressed consecutively in the RAM address space.

### RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 24 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

**REGISTER SUMMARY**

A register data format summary is shown in Figure 4.

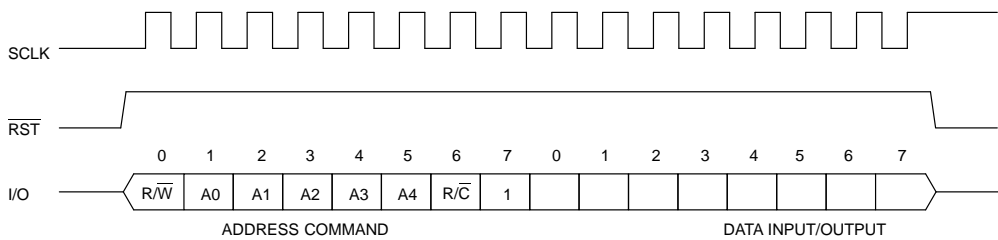
**CRYSTAL SELECTION**

A 32.768 KHz crystal, can be directly connected to the DS1202 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2

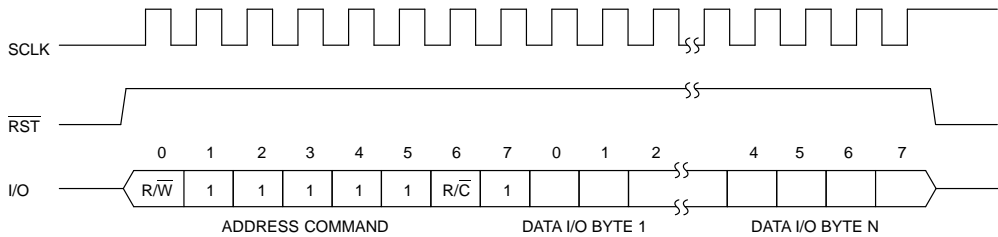
pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

**DATA TRANSFER SUMMARY** Figure 3

**SINGLE BYTE TRANSFER**



**BURST MODE TRANSFER**



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	$V_{CC}$	2.0		5.5	V	1
Logic 1 Input	$V_{IH}$	2.0		$V_{CC}+0.3$	V	1
Logic 0 Input	$V_{IL}$	$V_{CC}=2.0V$	-0.3	+0.3	V	1
		$V_{CC}=5V$	-0.3	+0.8		

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 2.0$  to 5.5V\*)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	$I_{LI}$			+500	$\mu A$	6
I/O Leakage	$I_{LO}$			+500	$\mu A$	6
Logic 1 Output	$V_{OH}$	$V_{CC}=2V$	1.6		V	2
		$V_{CC}=5V$	2.4			
Logic 0 Output	$V_{OL}$	$V_{CC}=2V$		0.4	V	3
		$V_{CC}=5V$		0.4		
Active Supply Current	$I_{CC}$	$V_{CC}=2V$		0.4	mA	5
		$V_{CC}=5V$		1.2		
Timekeeping Current	$I_{CC1}$	$V_{CC}=2V$		0.3	$\mu A$	4
		$V_{CC}=5V$		1		
Leakage Current	$I_{CC2}$	$V_{CC}=2V$		100	nA	10
		$V_{CC}=5V$		100		

\*Unless otherwise noted.

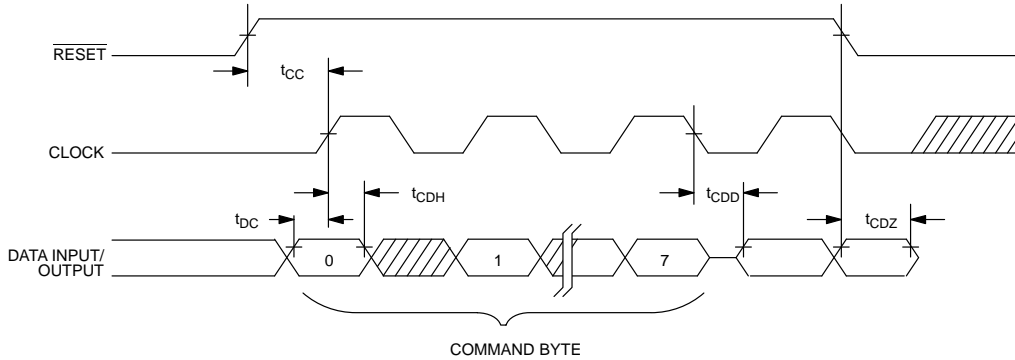
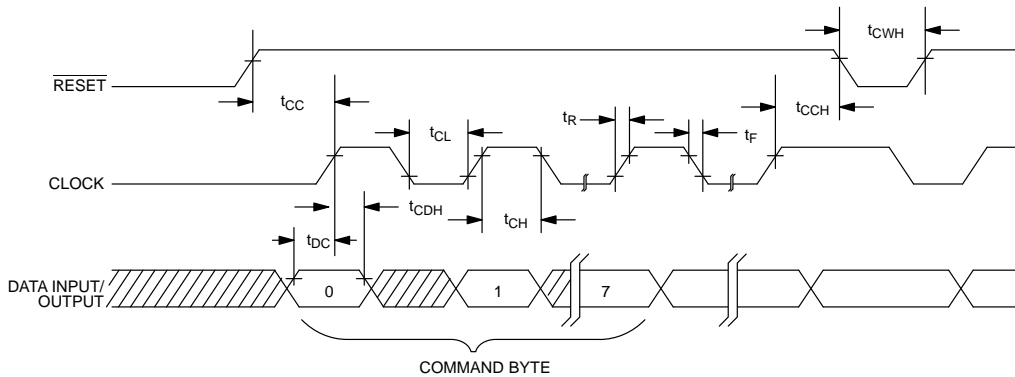
**CAPACITANCE** $(t_A = 25^\circ C)$ 

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_I$		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	$C_X$		6		pF	

**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 2.0$  to 5.5V\*)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	$t_{DC}$	$V_{CC}=2V$	200			ns 7
		$V_{CC}=5V$	50			
CLK to Data Hold	$t_{CDH}$	$V_{CC}=2V$	280			ns 7
		$V_{CC}=5V$	70			
CLK to Data Delay	$t_{CDD}$	$V_{CC}=2V$		800	ns	7, 8, 9
		$V_{CC}=5V$		200		
CLK Low Time	$t_{CL}$	$V_{CC}=2V$	1000		ns	7
		$V_{CC}=5V$	250			
CLK High Time	$t_{CH}$	$V_{CC}=2V$	1000		ns	7, 12
		$V_{CC}=5V$	250			
CLK Frequency	$f_{CLK}$	$V_{CC}=2V$		0.5	MHz	7, 12
		$V_{CC}=5V$	DC	2.0		
CLK Rise and Fall	$t_R, t_F$	$V_{CC}=2V$		2000	ns	
		$V_{CC}=5V$		500		
$\overline{RST}$ to CLK Setup	$t_{CC}$	$V_{CC}=2V$	4		$\mu s$	7
		$V_{CC}=5V$	1			
CLK to $\overline{RST}$ Hold	$t_{CCH}$	$V_{CC}=2V$	1000		ns	7
		$V_{CC}=5V$	250			
$\overline{RST}$ Inactive Time	$t_{CWH}$	$V_{CC}=2V$	4		$\mu s$	7
		$V_{CC}=5V$	1			
$\overline{RST}$ to I/O High Z	$t_{CDZ}$	$V_{CC}=2V$		280	ns	7
		$V_{CC}=5V$		70		

\*Unless otherwise noted.

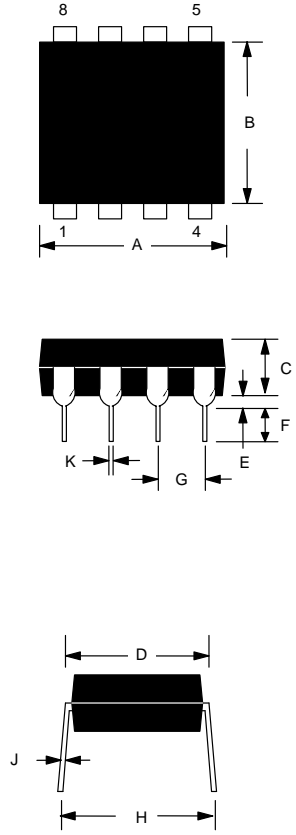
**TIMING DIAGRAM: READ DATA TRANSFER** Figure 5**TIMING DIAGRAM: WRITE DATA TRANSFER** Figure 6**NOTES:**

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at  $V_{CC}=5V$  and 0.4 mA at  $V_{CC}=2V$ ,  $V_{OH}=V_{CC}$  for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4 mA at  $V_{CC}=5V$  and 1.5 mA at  $V_{CC}=2V$ .
4.  $I_{CC1}$  is specified with I/O open,  $\overline{RST}$  set to a logic 0, and clock halt flag=0 (oscillator enabled).
5.  $I_{CC}$  is specified with the I/O pin open,  $\overline{RST}$  high,  $SCLK=2$  MHz at  $V_{CC}=5V$ ;  $SCLK=500$  KHz,  $V_{CC}=2V$  and clock halt flag=0 (oscillator enabled).
6.  $\overline{RST}$ ,  $SCLK$ , and I/O all have 40K $\Omega$  pull-down resistors to ground.
7. Measured at  $V_{IH}=2.0V$  or  $V_{IL}=0.8V$  and 10 ms maximum rise and fall time.
8. Measured at  $V_{OH}=2.4V$  or  $V_{OL}=0.4V$ .
9. Load capacitance = 50 pF.



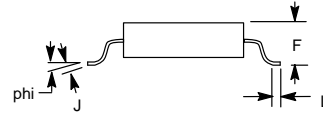
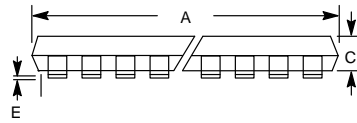
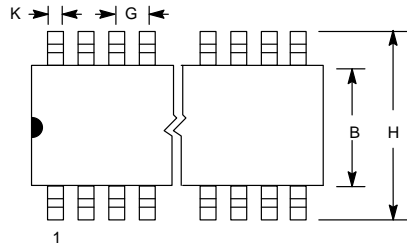
- 10.  $I_{CC2}$  is specified with  $\overline{RST}$ , I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
- 11. At power-up,  $\overline{RST}$  must be at a logic 0 until  $V_{CC} \geq 2$  volts. Also, SCLK must be at a logic 0 when  $\overline{RST}$  is driven to a logic one state.
- 12. If  $t_{CH}$  exceeds 100 ms with  $\overline{RST}$  in a logic one state, then  $I_{CC}$  may briefly exceed  $I_{CC}$  specification.

**DS1202 SERIAL TIMEKEEPER 8-PIN DIP**



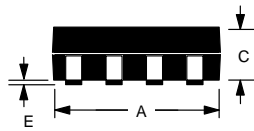
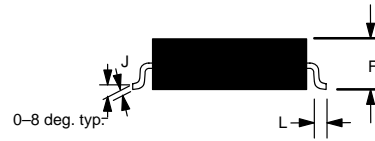
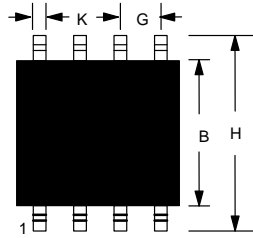
PKG	8-PIN	
	MIN	MAX
A IN. MM	0.360	0.400
B IN. MM	0.240	0.260
C IN. MM	0.120	0.140
D IN. MM	0.300	0.325
E IN. MM	0.015	0.040
F IN. MM	0.110	0.140
G IN. MM	0.090	0.110
H IN. MM	0.320	0.370
J IN. MM	0.008	0.012
K IN. MM	0.015	0.021

**DS1202S SERIAL TIMEKEEPER 16-PIN SOIC**



PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.500 12.70	0.511 12.99
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.20
phi	0°	8°

**DS1202S8 8-PIN SOIC 200 MIL**



PKG	8-PIN	
	DIM	MIN
A IN. MM	0.203 5.16	0.213 5.41
B IN. MM	0.203 5.16	0.213 5.41
C IN. MM	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.102	0.010 0.390
F IN. MM	0.074 1.88	0.84 2.13
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.302 7.67	0.318 8.07
J IN. MM	0.006 0.152	0.010 0.254
K IN. MM	0.013 0.33	0.020 0.508
L IN. MM	0.19 4.83	0.030 0.762