

# CD74HC137, CD74HCT137, CD74HC237, CD74HCT237

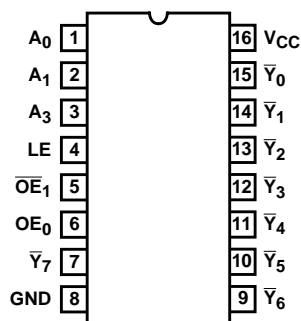
## High Speed CMOS Logic, 3-to-8 Line Decoder Demultiplexer with Address Latches

### Features

- Select One of Eight Data Outputs
  - Active Low for CD74HC137 and CD74HCT137
  - Active High for CD74HC237 and CD74HCT237
- I/O Port or Memory Selector
- Two Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13ns at  $V_{CC} = 5V$ ,  
15pF,  $T_A = 25^\circ C$  (CD74HC237)
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL  
Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$ , of  $V_{CC}$   
at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  
 $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Pinout

CD74HC137, CD74HCT137, CD74HC237, CD74HCT237  
(PDIP, SOIC)  
TOP VIEW



### **Description**

The Harris CD74HC137, CD74HC237 and CD74HCT137, CD74HCT237 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

Both circuits have three binary select inputs (A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub>) that can be latched by an active High Latch Enable (LE) signal to isolate the outputs from select-input changes. A "Low" LE makes the output transparent to the input and the circuit functions as a one-of-eight decoder. Two Output Enable inputs ( $\overline{OE}_1$  and OE<sub>0</sub>) are provided to simplify cascading and to facilitate demultiplexing. The demultiplexing function is accomplished by using the A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub> inputs to select the desired output and using one of the other Output Enable inputs as the data input while holding the other Output Enable input in its active state. In the CD74HC137 and CD74HCT137 the selected output is a "Low"; in the CD74HC237 and CD74HCT237 the selected output is a "High".

### **Ordering Information**

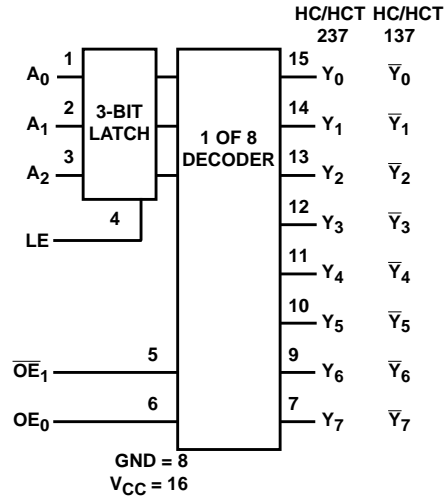
<b>PART NUMBER</b>	<b>TEMP. RANGE (°C)</b>	<b>PACKAGE</b>	<b>PKG. NO.</b>
CD74HC137E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT137E	-55 to 125	16 Ld PDIP	E16.3
CD74HC237E	-55 to 125	16 Ld PDIP	E16.3
CD74HC237M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT237E	-55 to 125	16 Ld PDIP	E16.3

**NOTES:**

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

**CD74HC137, CD74HCT137, CD74HC237, CD74HCT237**

**Functional Diagram**



**CD74HC137, CD74HCT137 TRUTH TABLE**

INPUTS						OUTPUTS							
LE	OE <sub>0</sub>	OE <sub>1</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Y <sub>0</sub> <sup>bar</sup>	Y <sub>1</sub> <sup>bar</sup>	Y <sub>2</sub> <sup>bar</sup>	Y <sub>3</sub> <sup>bar</sup>	Y <sub>4</sub> <sup>bar</sup>	Y <sub>5</sub> <sup>bar</sup>	Y <sub>6</sub> <sup>bar</sup>	Y <sub>7</sub> <sup>bar</sup>
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

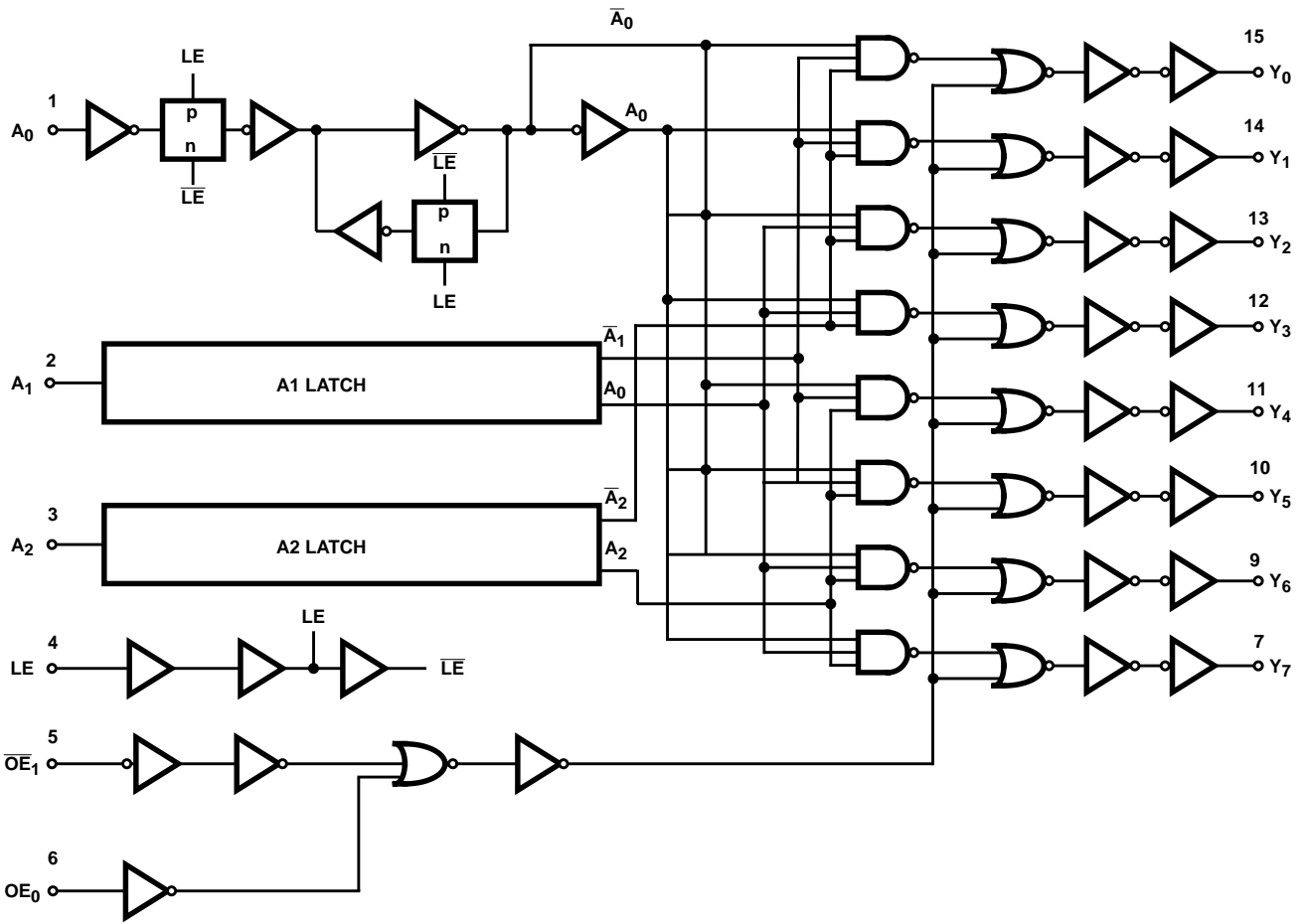
NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

**CD74HC237, CD74HCT237 TRUTH TABLE**

INPUTS						OUTPUTS							
LE	OE <sub>0</sub>	OE <sub>1</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

**Functional Block Diagram**



# CD74HC137, CD74HCT137, CD74HC237, CD74HCT237

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	160
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	$.2V$ to $6V$
HCT Types .....	$4.5V$ to $5.5V$
DC Input or Output Voltage, $V_I, V_O$ .....	$0V$ to $V_{CC}$
Input Rise and Fall Time	
$2V$ .....	$1000ns$ (Max)
$4.5V$ .....	$500ns$ (Max)
$6V$ .....	$400ns$ (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

**CD74HC137, CD74HCT137, CD74HC237, CD74HCT237**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
All	1.5

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**Prerequisite For Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
A <sub>n</sub> to LE Setup Time	t <sub>SU</sub>	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
A <sub>n</sub> to LE Hold Time	t <sub>H</sub>	2	30	-	-	40	-	45	-	ns
		4.5	6	-	-	8	-	9	-	ns
		6	5	-	-	7	-	8	-	ns

**CD74HC137, CD74HCT137, CD74HC237, CD74HCT237**

**Prerequisite For Switching Specifications (Continued)**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
LE Pulse Width	t <sub>W</sub>	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	1	-	13	-	ns
<b>HCT TYPES</b>										
An to LE Setup Time	t <sub>SU</sub>	4.5	10	-	-	13	-	15	-	ns
An to LE Hold Time	t <sub>H</sub>	4.5	7	-	-	9	-	11	-	ns
		CD74HCT237	t <sub>H</sub>	4.5	5	-	-	5	-	5
LE Pulse Width	t <sub>W</sub>	4.5	10	-	-	13	-	15	-	ns

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay CD74HC137, CD74HCT137 An to any $\bar{Y}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			6	-	-	31	-	38	-	46	ns
Propagation Delay CD74HC237, CD74HCT237 An to any Y	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
			6	-	-	27	-	34	-	41	ns
Address to Output CD74HC137	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	5	15	-	-	-	-	-	ns
			CD74HC237	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	13	-	-	-
OE <sub>0</sub> to any $\bar{Y}$ or Y	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
			6	-	-	25	-	31	-	38	ns
OE <sub>1</sub> to any $\bar{Y}$ or Y	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
			6	-	-	25	-	31	-	38	ns
LE to any $\bar{Y}$ or Y	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
			6	-	-	32	-	41	-	48	ns
Power Dissipation Capacitance, (Notes 4, 5)	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	-	19	-	-	-	-	-	pF
			CD74HC237	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	-	23	-	-	-
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>I</sub>	-	-	-	-	-	-	-	-	10 pF	

# CD74HC137, CD74HCT137, CD74HC237, CD74HCT237

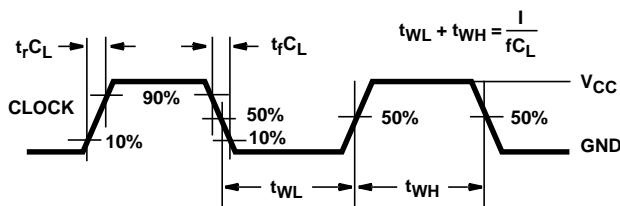
## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>											
Propagation Delay An to any $\bar{Y}$ or Y Address to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	38	-	48	-	57	ns
	$t_{PLH}, t_{PHL}$	$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
$OE_0$ to any Y (HC137)	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
$OE_0$ to any $\bar{Y}$ (HC237)	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	33	-	41	-	60	ns
$\bar{OE}_1$ to any $\bar{Y}$ (HC137)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	37	-	46	-	56	ns
$\bar{OE}_1$ to any $\bar{Y}$ (HC237)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
LE to any Y (HC137)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	44	-	55	-	66	ns
LE to any $\bar{Y}$ (HC237)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
Power Dissipation Capacitance, (Notes 4, 5)											
	CD74HC137	$C_{PD}$	$C_L = 15\text{pF}$	5	-	19	-	-	-	-	pF
	CD74HC237	$C_{PD}$	$C_L = 15\text{pF}$	5	-	23	-	-	-	-	pF
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5			15		19		22	ns
Input Capacitance	$C_i$	-	-	-	-	10	-	10	-	10	pF

**NOTES:**

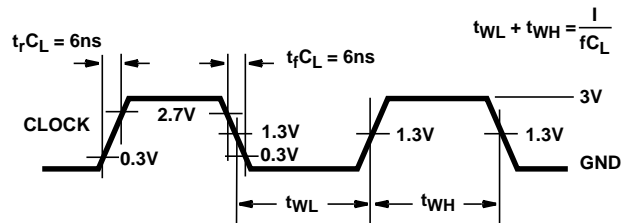
- $C_{PD}$  is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where:  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



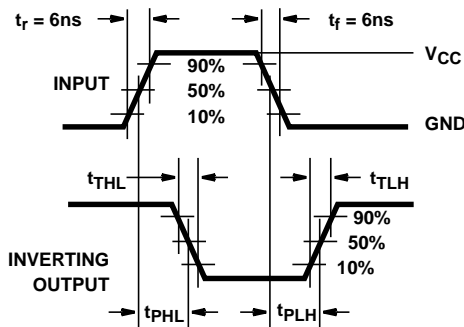
NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

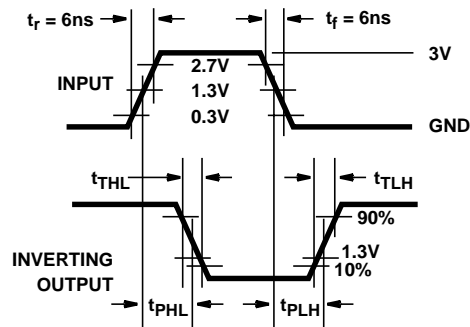


NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



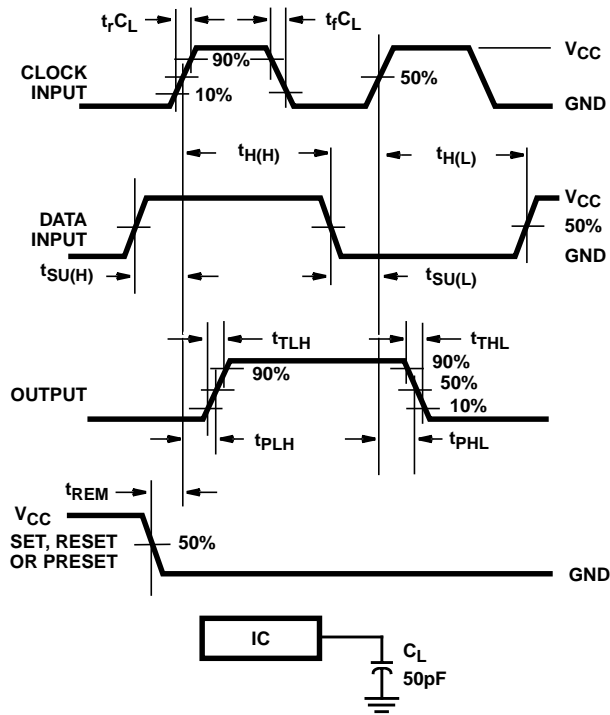
**FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



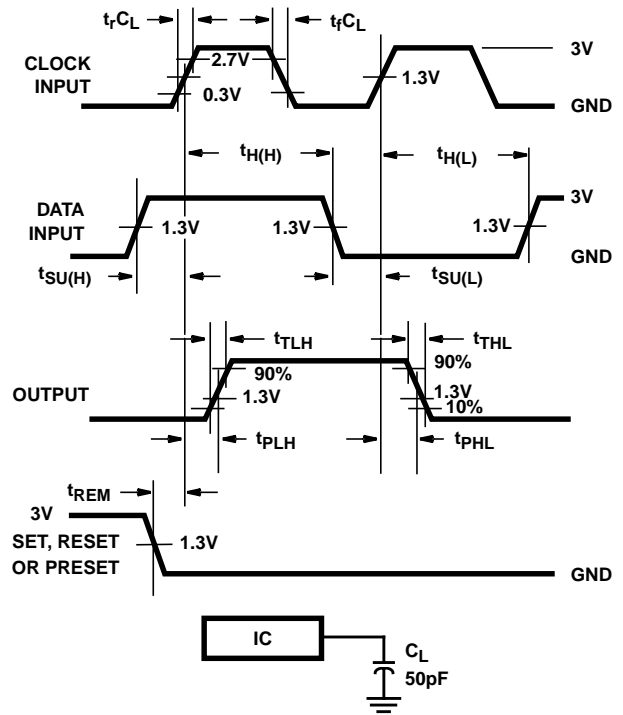
**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**Test Circuits and Waveforms (Continued)**



**FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**



**FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

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