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Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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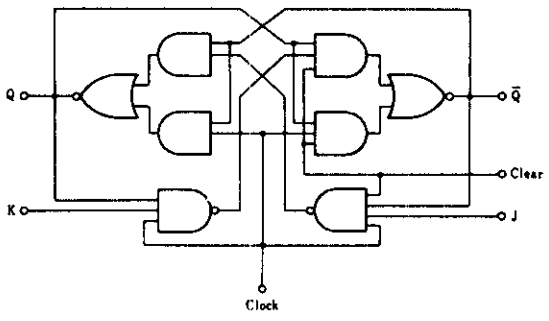
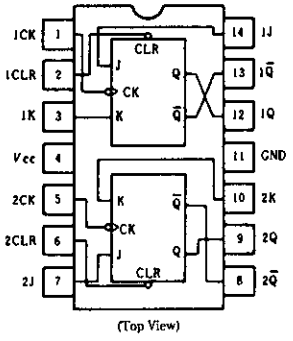
HD74LS73A ●Dual J-K Flip-Flops (with Clear)

■BLOCK DIAGRAM(½)



■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Inputs				Outputs	
Clear	Clock	J	K	Q	$\bar{Q}$
L	×	×	×	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	×	×	Q_0	$\bar{Q}_0$

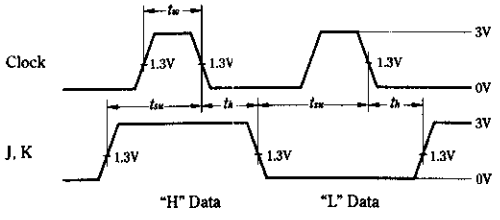
Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
Q_0; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of $\bar{Q}0$ or level of Q before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

■RECOMMENDED OPERATING CONDITION

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	—	30	MHz
Pulse width	Clock High	t_w	20	—	—	ns
	Clear Low		25	—	—	
Setup time	"H" Data	t_{su}	20↓	—	—	ns
	"L" Data		20↓	—	—	
Hold time		t_h	0↓	—	—	ns

Note) ↓; The arrow indicates the falling edge.

■TIMING DEFINITION



■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	—	—	V
		V_{IL}			—	—	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	—	—	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=8mA$	—	—	0.5	V
				$I_{OL}=4mA$	—	—	0.4	
Input current	J, K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	Clear				—	—	60	
	Clock				—	—	80	
	J, K	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	Clear				—	—	0.8	
	Clock				—	—	−0.8	
	J, K	I_I	$V_{CC}=5.25V$, $V_I=7V$		—	—	0.1	mA
	Clear				—	—	0.3	
	Clock				—	—	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	—	−100	mA
Supply current **		I_{CC}	$V_{CC}=5.25V$		—	4	6	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

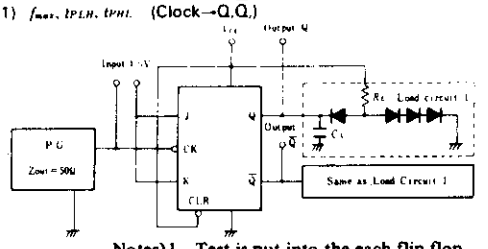
■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	30	45	—	MHz
Propagation delay time	t_{PLH}	Clear	Q, $\bar{Q}$		—	15	20	ns
	t_{PHL}	Clock			—	15	20	ns

■TESTING METHOD

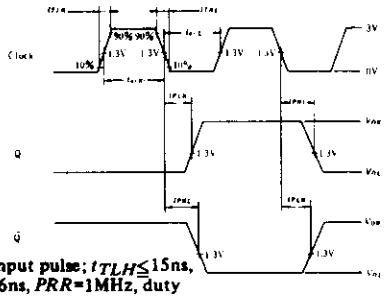
1) Test Circuit

1.1) f_{max}, t_{PLH}, t_{PHL} (Clock→Q, $\bar{Q}$)



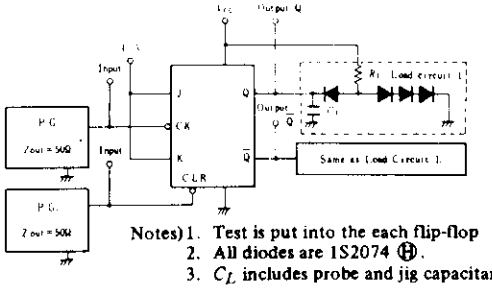
Notes) 1. Test is put into the each flip flop
2 All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

Waveform



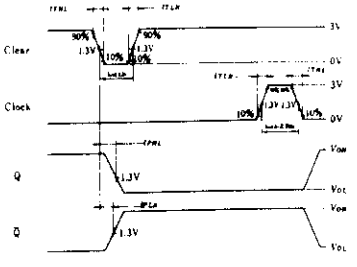
Note) Clock input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$, duty cycle=50% and: for f_{max}, $t_{TLH}=t_{THL} \leq 2.5ns$.

1.2) t_{PHL} (Clear→Q), t_{PLH} (Clear→$\bar{Q}$)



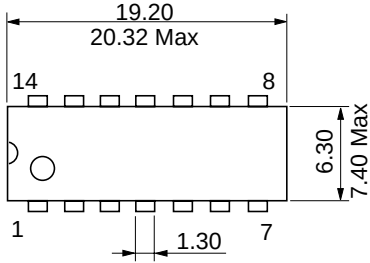
Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

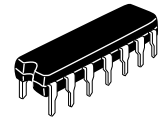
Waveform

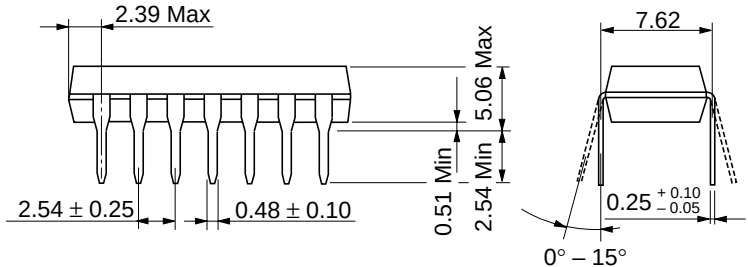


Note) Clear and clock input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$

Unit: mm

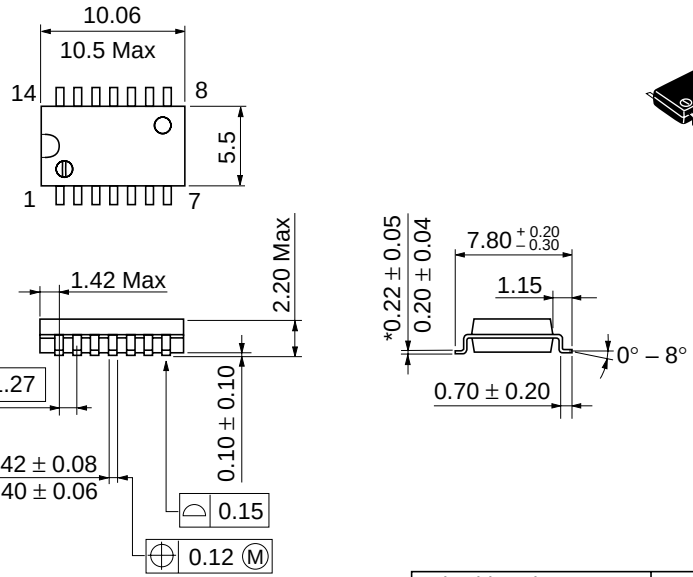


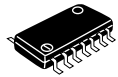




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

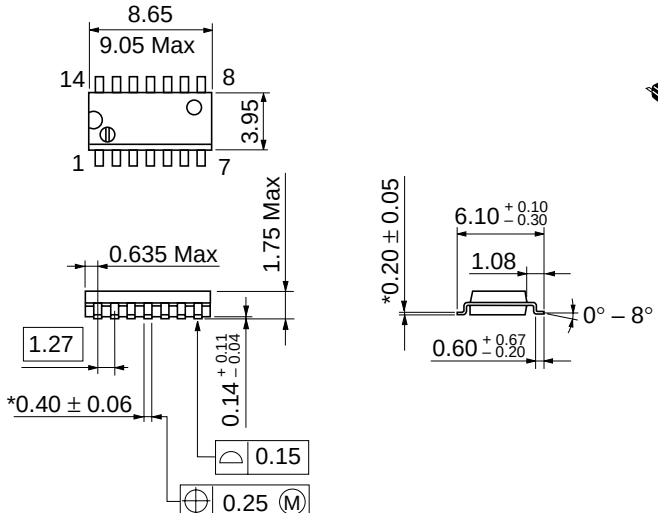




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX