FAIRCHILD SEMICONDUCTOR™

November 1988
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74AC14
Hex Inverter with Schmitt Trigger Input

General Description

The AC14 contains six inverter gates each with a Schmitt trigger input. The AC14 contains six logic inverters which accept standard CMOS input signals and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The AC14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

- I_{CC} reduced by 50%
- Outputs source/sink 24 mA

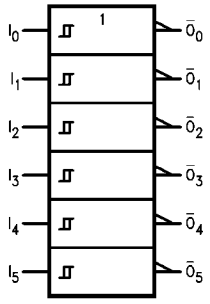
Ordering Code:

Order Number	Package Number	Package Description
74AC14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74AC14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

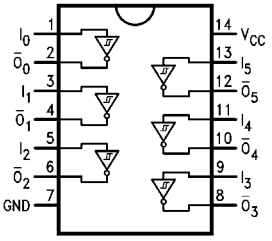
Logic Symbol

IEEE/IEC



Connection Diagram

Pin Assignment for DIP, SOIC and TSSOP



Pin Descriptions

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Function Table

Input	Output
A	$\overline{O}$
L	H
H	L

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
PDIP	−40°C to +85°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -55°C$ to $+125°C$ Guaranteed Limits	$T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50$ µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$I_{OH} = 12$
		4.5		3.86	3.76		$I_{OH} = 24$ mA
		5.5		4.86	4.76		$I_{OH} = 24$ mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50$ µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.5	0.44	V
		4.5		0.36	0.5	0.44	I_{OL} 24 mA
		5.5		0.36	0.5	0.44	$I_{OL} = 24$ mA (Note 2)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	µA $V_I = V_{CC}$, GND
V_{t+}	Maximum Positive Threshold	3.0		2.2	2.2	2.2	V T_A = Worst Case
		4.5		3.2	3.2	3.2	
		5.5		3.9	3.9	3.9	
V_{t-}	Minimum Negative Threshold	3.0		0.5	0.5	0.5	V T_A = Worst Case
		4.5		0.9	0.9	0.9	
		5.5		1.1	1.1	1.1	
$V_{h(max)}$	Maximum Hysteresis	3.0		1.2	1.2	1.2	V T_A = Worst Case
		4.5		1.4	1.4	1.4	
		5.5		1.6	1.6	1.6	
$V_{h(min)}$	Minimum Hysteresis	3.0		0.3	0.3	0.3	V T_A = Worst Case
		4.5		0.4	0.4	0.4	
		5.5		0.5	0.5	0.5	
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			50	75	mA $V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−50	−75	mA $V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		2.0	40.0	20.0	µA $V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics (Continued)

AC Electrical Characteristics

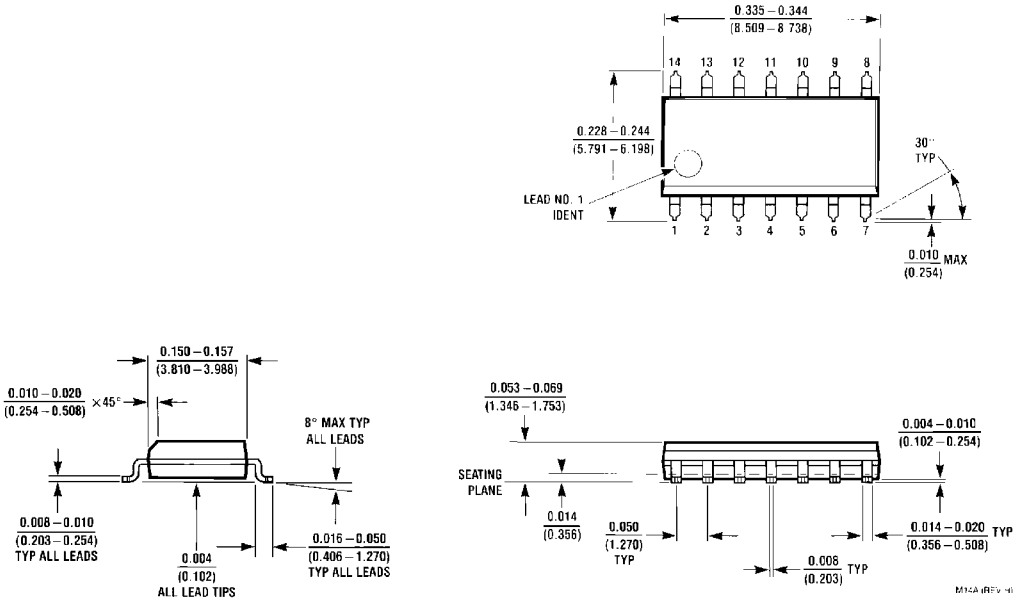
Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.0	16.0	1.5	15.0	ns
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0	
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.0	14.0	1.5	13.0	ns
		5.0	1.5	6.0	8.5	1.5	10.0	1.5	9.5	

Note 5: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

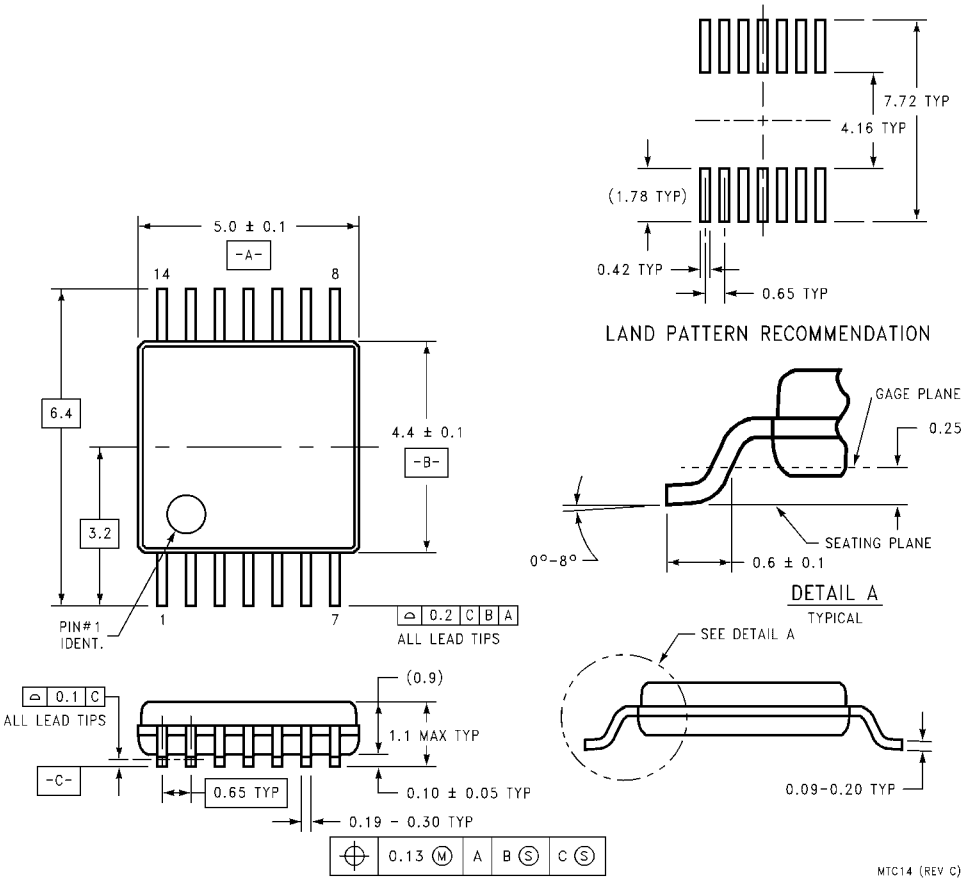
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	25.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



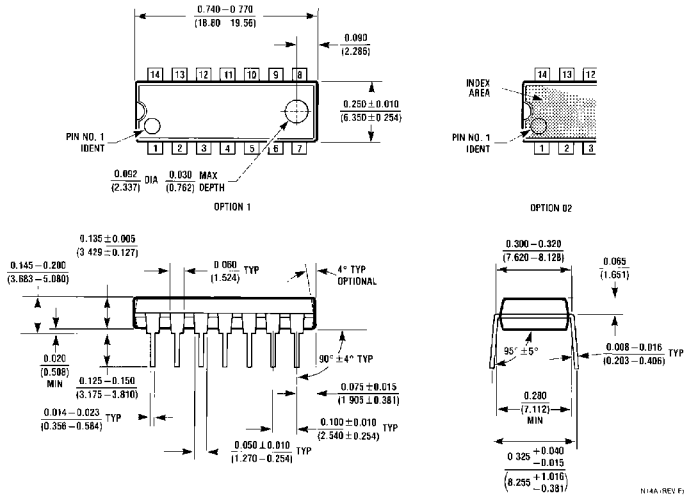
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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