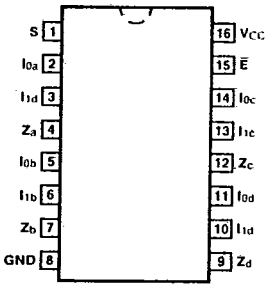
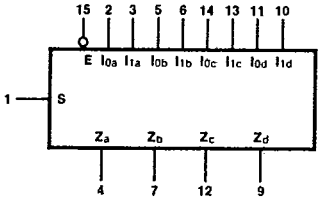
54/74157
54S/74S157
54LS/74LS157
QUAD 2-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '157 is a high speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The '157 can also be used to generate any four of the 16 different functions to two variables.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74157PC, 74S157PC 74LS157PC		9B
Ceramic DIP (D)	A	74157DC, 74S157DC 74LS157DC	54157DM, 54S157DM 54LS157DM	6B
Flatpak (F)	A	74157FC, 74S157FC 74LS157FC	54157FM, 54S157FM 54LS157FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

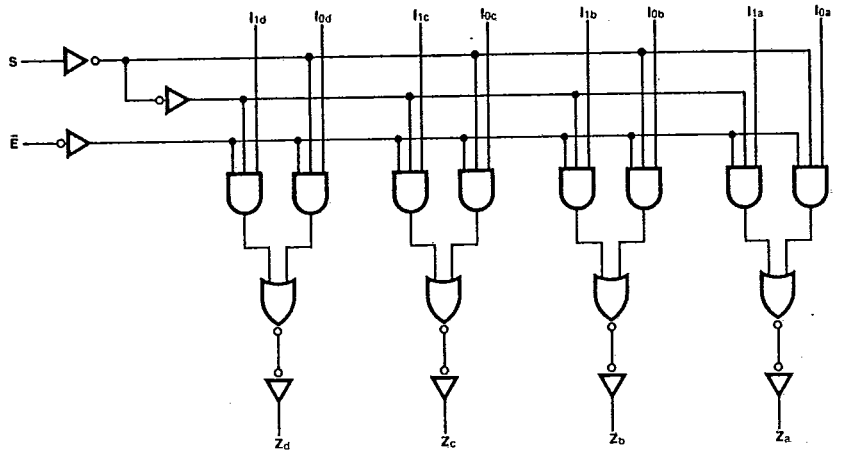
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{0d}	Source 0 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
I_{1a} — I_{1d}	Source 1 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	2.5/2.5	1.0/0.5
S	Select Input	1.0/1.0	2.5/2.5	1.0/0.5
Z_a — Z_d	Outputs	20/10	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The '157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

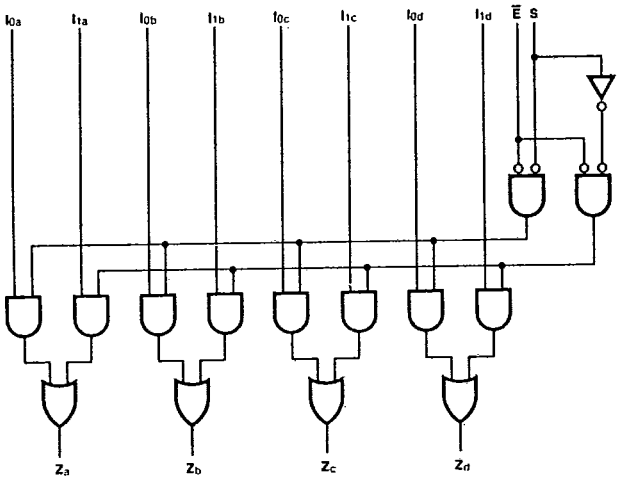
$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the '157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The '157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

LOGIC DIAGRAMS
'157



'S157 • 'LS157



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TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-40	-100	-20	-100		
I_{CC}	Power Supply Current			48		78		16	mA	V_{CC} = Max All Inputs = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to Z_n		23 27		15 15		26 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n		20 21		12.5 12		20 21	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		14 14		7.5 6.5		14 14	ns	Figs. 3-1, 3-5